■ FEATURES

- Direct display of RAM data through the display data RAMS.
- RAM capacity：64 x 64 = 4096 bits
- Display duty selectable by software
  1/64 duty：64common x 128segment (RW1065I x 2)
  64common x 192segment (RW1065I x 3)
  1/32 duty：32common x 128segment (RW1065I x 2)
  32common x 192segment (RW1065I x 3)

- **RW1065I can support High-speed IIC interface and 4-line serial interface**
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all point ON/OFF, read/modify/write, segment driver direction selects, power saver.
- Low-power liquid crystal display power supply circuit equipped internally.
- Bias set 1/5 1/6 1/8 1/9 by pin.
- Booster circuit (with Boost ratios of 2X/3X/4X, where the step-up voltage reference power supply can be input externally).
  V_0 voltage regulator resistors equipped externally, V_1 to V_4 voltage divider resistors equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Low power consumption.
  Logic power supply $V_{DD} – V_{SS}$ = 2.7V to 5.5 V
  Boost reference voltage: $V_{DD2} – V_{SS}$ = 2.7V to 5.5V
  Booster maximum voltage limited V_{OUT}=17.0V
  Liquid crystal drive power supply:
  $V_0 – V_{SS}$ = 4.0V to 15.0 V
- Wide range of operating temperatures: –40 to 85℃
- CMOS process.
- Shipping forms include bare chip and COB.
- Software compatible to KS0108.

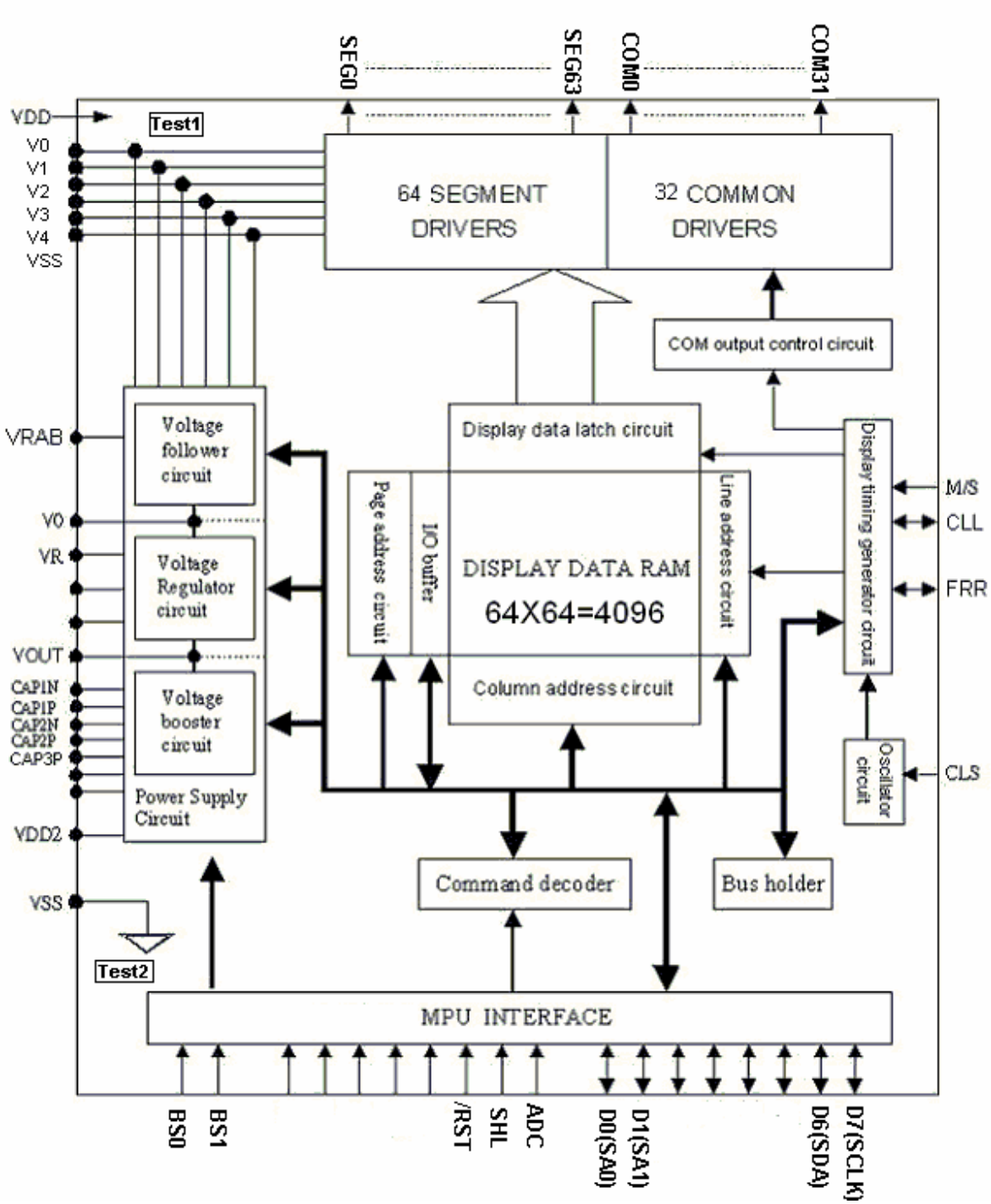
■ GENERAL DESCRIPTION

The RW1065I is a single-chip dot matrix LCD driver that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and generates liquid crystal drive signal independently of the microprocessor. Because the chips in the RW1065I contain 64x64 bits of display data RAM and there is a 1-to-1 correspondence between the LCD panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.
The RW1065I chips contain 32 common output circuits and 64 segment output circuits, so that two RW1065I chips can drive a 64x128 dot display (capable of displaying 8 columnsx4 rows of a 16x16 dot kanji font).
Moreover, the capacity of the display can be extended through the use of master/slave structures up to three RW1065I chips.
The RW1065I chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power LCD driver power supply, and a display clock CR oscillator circuit, the RW1065I can be used to create the lowest power display system with the fewest components for high-performance portable devices.

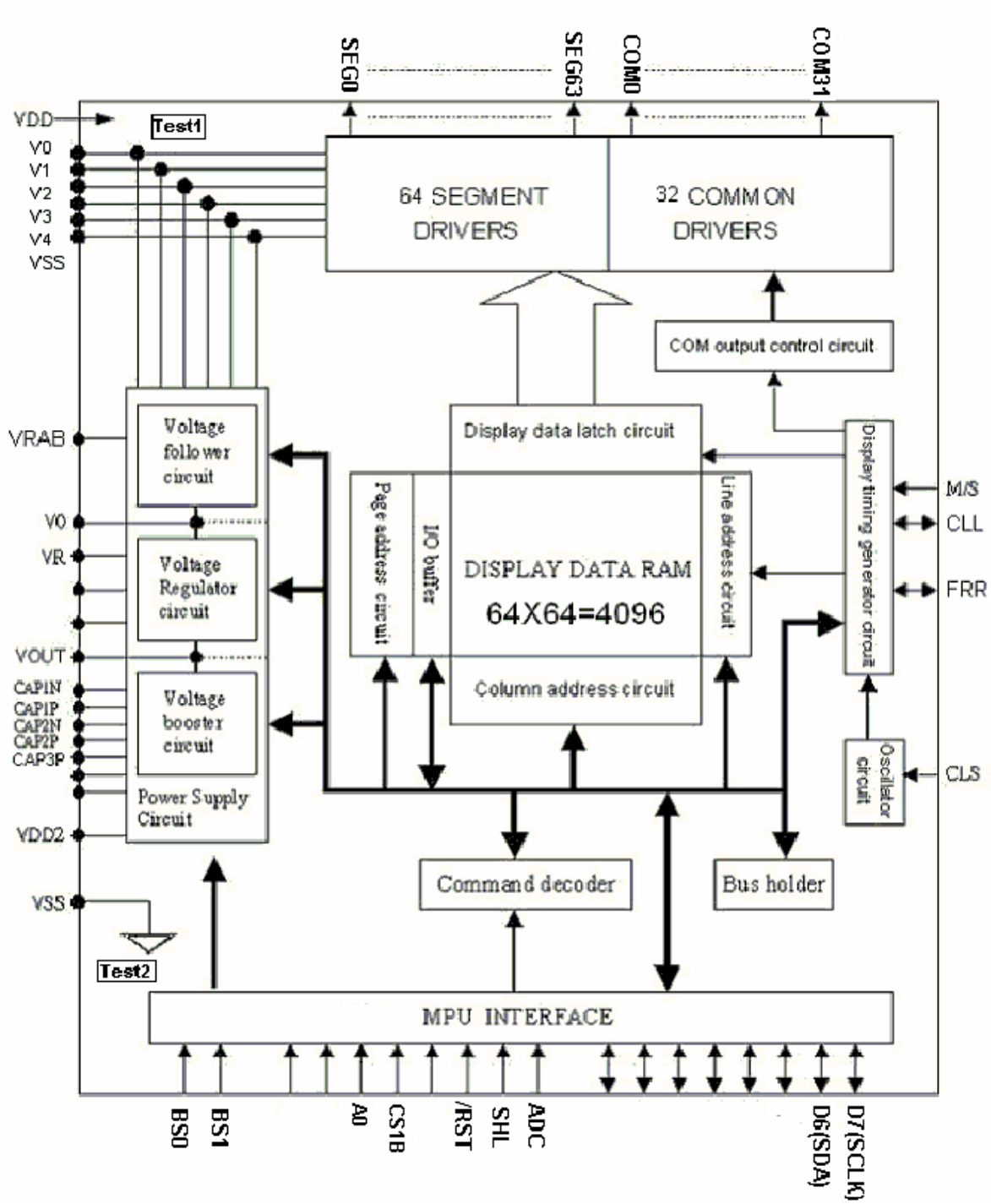
RW1065I Series Revision History		
Version	**Date**	**Description**
V0.0	2011/8/15	First Edition

■ BLOCK DIAGRAM

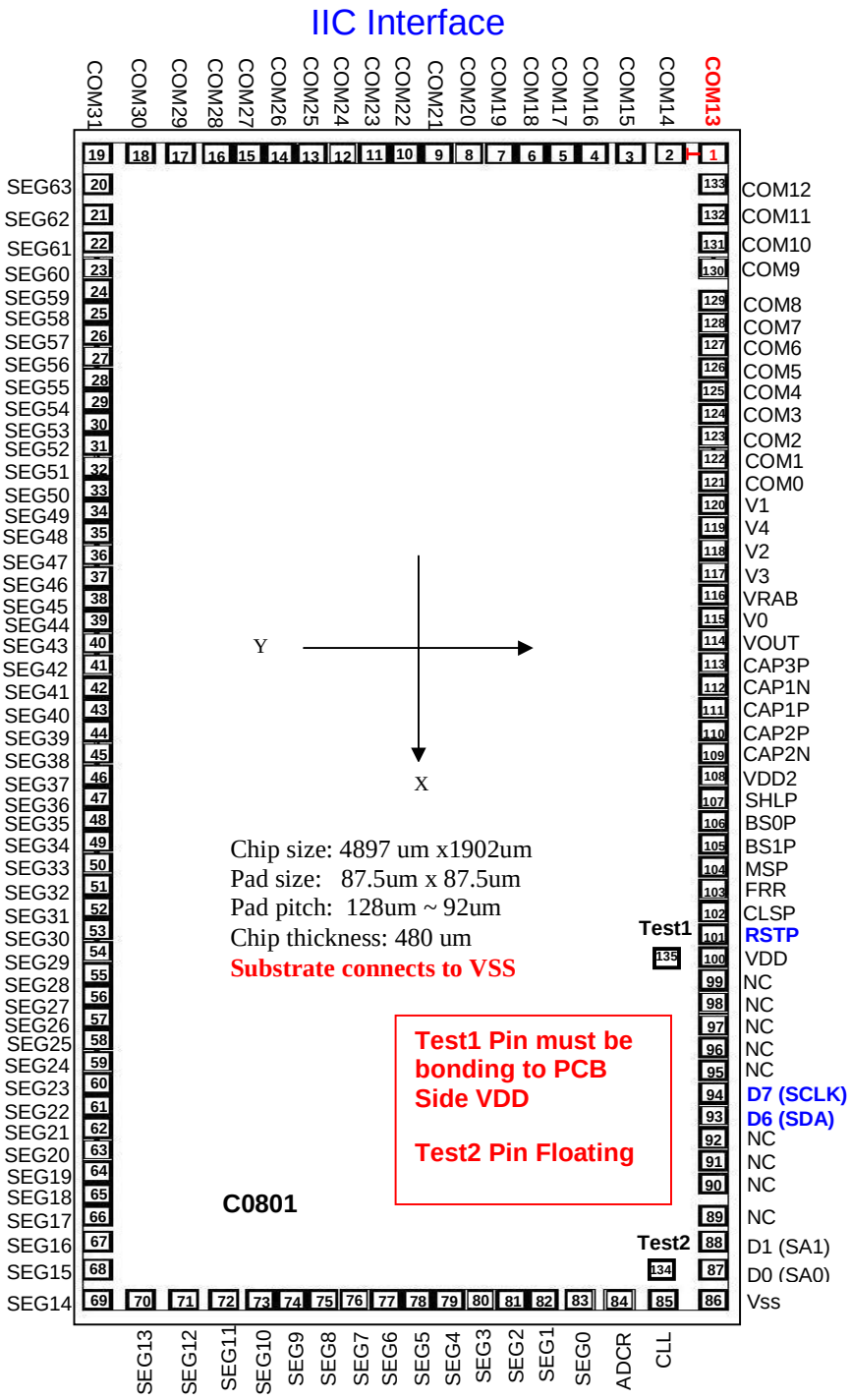
IIC Interface



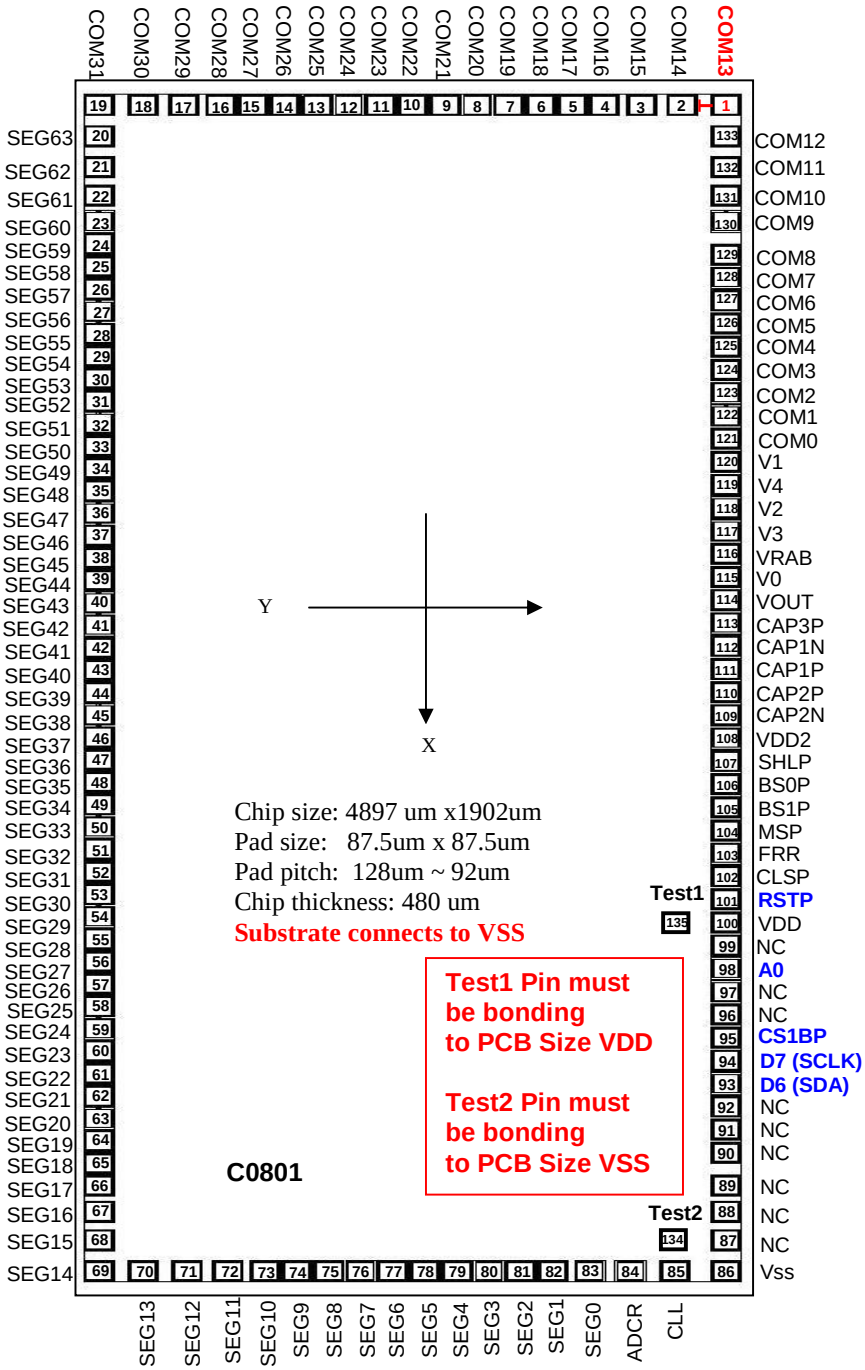
4-SPI Interface



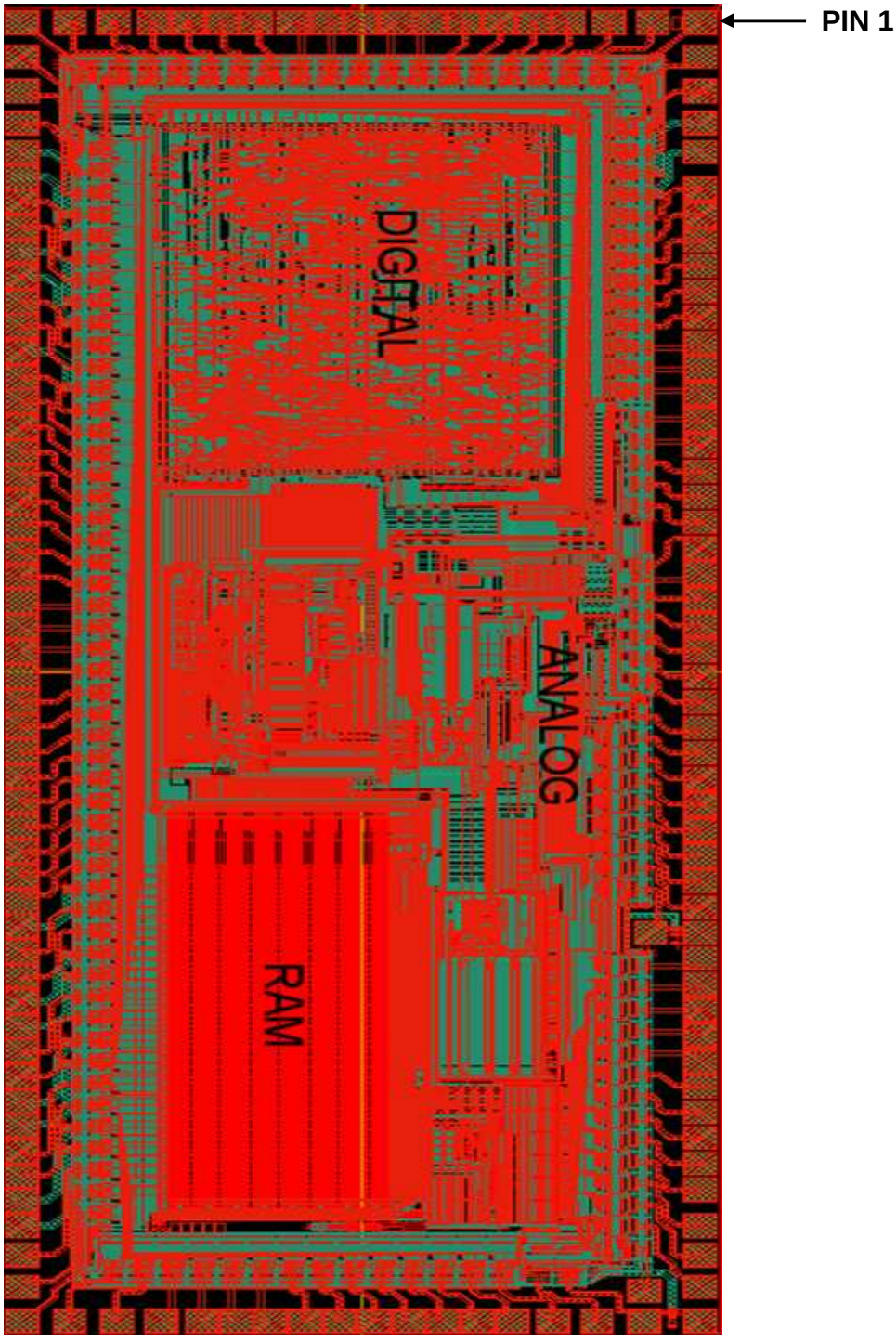
■ PAD ARRANGEMENT



4-SPI Interface



■ CHIP LAYOUT



■ PAD CENTER COORDINATES (IIC Interface)

DUTY=1/64 duty, SHL=0, SHLA=X

Pad	Pin Name		X	Y
	Master	Slave		
1	COM13	COM45	-2404.75	907.25
2	COM14	COM46	-2404.75	779.75
3	COM15	COM47	-2404.75	662.25
4	COM16	COM48	-2404.75	554.75
5	COM17	COM49	-2404.75	462.75
6	COM18	COM50	-2404.75	370.25
7	COM19	COM51	-2404.75	277.75
8	COM20	COM52	-2404.75	185.25
9	COM21	COM53	-2404.75	92.75
10	COM22	COM54	-2404.75	0.25
11	COM23	COM55	-2404.75	-92.25
12	COM24	COM56	-2404.75	-184.75
13	COM25	COM57	-2404.75	-277.25
14	COM26	COM58	-2404.75	-369.75
15	COM27	COM59	-2404.75	-462.25
16	COM28	COM60	-2404.75	-554.75
17	COM29	COM61	-2404.75	-662.25
18	COM30	COM62	-2404.75	-779.75
19	COM31	COM63	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	D0(SA0)	2277.25	907.25
88	D1(SA1)	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	NC		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	NC		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM0	COM32	-1028.5	907.25
122	COM1	COM33	-1123.5	907.25
123	COM2	COM34	-1218.5	907.25
124	COM3	COM35	-1313.5	907.25
125	COM4	COM36	-1408.5	907.25
126	COM5	COM37	-1503.5	907.25
127	COM6	COM38	-1598.5	907.25
128	COM7	COM39	-1693.5	907.25
129	COM8	COM40	-1788.5	907.25
130	COM9	COM41	-1924.75	907.25
131	COM10	COM42	-2032.25	907.25
132	COM11	COM43	-2149.75	907.25
133	COM12	COM44	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ PAD CENTER COORDINATES (IIC Interface)

DUTY=1/64 duty, SHL=1, SHLA=0

Pad	Pin Name		X	Y
	Master	Slave		
1	COM50	COM18	-2404.75	907.25
2	COM49	COM17	-2404.75	779.75
3	COM48	COM16	-2404.75	662.25
4	COM47	COM15	-2404.75	554.75
5	COM46	COM14	-2404.75	462.75
6	COM45	COM13	-2404.75	370.25
7	COM44	COM12	-2404.75	277.75
8	COM43	COM11	-2404.75	185.25
9	COM42	COM10	-2404.75	92.75
10	COM41	COM9	-2404.75	0.25
11	COM40	COM8	-2404.75	-92.25
12	COM39	COM7	-2404.75	-184.75
13	COM38	COM6	-2404.75	-277.25
14	COM37	COM5	-2404.75	-369.75
15	COM36	COM4	-2404.75	-462.25
16	COM35	COM3	-2404.75	-554.75
17	COM34	COM2	-2404.75	-662.25
18	COM33	COM1	-2404.75	-779.75
19	COM32	COM0	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	D0(SA0)	2277.25	907.25
88	D1(SA1)	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	NC		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	NC		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM63	COM31	-1028.5	907.25
122	COM62	COM30	-1123.5	907.25
123	COM61	COM29	-1218.5	907.25
124	COM60	COM28	-1313.5	907.25
125	COM59	COM27	-1408.5	907.25
126	COM58	COM26	-1503.5	907.25
127	COM57	COM25	-1598.5	907.25
128	COM56	COM24	-1693.5	907.25
129	COM55	COM23	-1788.5	907.25
130	COM54	COM22	-1924.75	907.25
131	COM53	COM21	-2032.25	907.25
132	COM52	COM20	-2149.75	907.25
133	COM51	COM19	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ PAD CENTER COORDINATES (IIC Interface)

DUTY=1/64 duty, SHL=1, SHLA=1

Pad	Pin Name		X	Y
	Master	Slave		
1	COM18	COM50	-2404.75	907.25
2	COM17	COM49	-2404.75	779.75
3	COM16	COM48	-2404.75	662.25
4	COM15	COM47	-2404.75	554.75
5	COM14	COM46	-2404.75	462.75
6	COM13	COM45	-2404.75	370.25
7	COM12	COM44	-2404.75	277.75
8	COM11	COM43	-2404.75	185.25
9	COM10	COM42	-2404.75	92.75
10	COM9	COM41	-2404.75	0.25
11	COM8	COM40	-2404.75	-92.25
12	COM7	COM39	-2404.75	-184.75
13	COM6	COM38	-2404.75	-277.25
14	COM5	COM37	-2404.75	-369.75
15	COM4	COM36	-2404.75	-462.25
16	COM3	COM35	-2404.75	-554.75
17	COM2	COM34	-2404.75	-662.25
18	COM1	COM33	-2404.75	-779.75
19	COM0	COM32	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	D0(SA0)	2277.25	907.25
88	D1(SA1)	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	NC		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	NC		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM31	COM63	-1028.5	907.25
122	COM30	COM62	-1123.5	907.25
123	COM29	COM61	-1218.5	907.25
124	COM28	COM60	-1313.5	907.25
125	COM27	COM59	-1408.5	907.25
126	COM26	COM58	-1503.5	907.25
127	COM25	COM57	-1598.5	907.25
128	COM24	COM56	-1693.5	907.25
129	COM23	COM55	-1788.5	907.25
130	COM22	COM54	-1924.75	907.25
131	COM21	COM53	-2032.25	907.25
132	COM20	COM52	-2149.75	907.25
133	COM19	COM51	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ PAD CENTER COORDINATES (IIC Interface)

DUTY=1/32 duty, SHL=0, SHLA=X

Pad	Pin Name		X	Y
	Master	Slave		
1	COM13	COM29	-2404.75	907.25
2	COM14	COM30	-2404.75	779.75
3	COM15	COM31	-2404.75	662.25
4	COM16	COM0	-2404.75	554.75
5	COM17	COM1	-2404.75	462.75
6	COM18	COM2	-2404.75	370.25
7	COM19	COM3	-2404.75	277.75
8	COM20	COM4	-2404.75	185.25
9	COM21	COM5	-2404.75	92.75
10	COM22	COM6	-2404.75	0.25
11	COM23	COM7	-2404.75	-92.25
12	COM24	COM8	-2404.75	-184.75
13	COM25	COM9	-2404.75	-277.25
14	COM26	COM10	-2404.75	-369.75
15	COM27	COM11	-2404.75	-462.25
16	COM28	COM12	-2404.75	-554.75
17	COM29	COM13	-2404.75	-662.25
18	COM30	COM14	-2404.75	-779.75
19	COM31	COM15	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	D0(SA0)	2277.25	907.25
88	D1(SA1)	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	NC		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	NC		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM0	COM16	-1028.5	907.25
122	COM1	COM17	-1123.5	907.25
123	COM2	COM18	-1218.5	907.25
124	COM3	COM19	-1313.5	907.25
125	COM4	COM20	-1408.5	907.25
126	COM5	COM21	-1503.5	907.25
127	COM6	COM22	-1598.5	907.25
128	COM7	COM23	-1693.5	907.25
129	COM8	COM24	-1788.5	907.25
130	COM9	COM25	-1924.75	907.25
131	COM10	COM26	-2032.25	907.25
132	COM11	COM27	-2149.75	907.25
133	COM12	COM28	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ PAD CENTER COORDINATES (IIC Interface)

DUTY=1/32 duty, SHL=1, SHLA=X

Pad	Pin Name		X	Y
	Master	Slave		
1	COM18	COM2	-2404.75	907.25
2	COM17	COM1	-2404.75	779.75
3	COM16	COM0	-2404.75	662.25
4	COM15	COM31	-2404.75	554.75
5	COM14	COM30	-2404.75	462.75
6	COM13	COM29	-2404.75	370.25
7	COM12	COM28	-2404.75	277.75
8	COM11	COM27	-2404.75	185.25
9	COM10	COM26	-2404.75	92.75
10	COM9	COM25	-2404.75	0.25
11	COM8	COM24	-2404.75	-92.25
12	COM7	COM23	-2404.75	-184.75
13	COM6	COM22	-2404.75	-277.25
14	COM5	COM21	-2404.75	-369.75
15	COM4	COM20	-2404.75	-462.25
16	COM3	COM19	-2404.75	-554.75
17	COM2	COM18	-2404.75	-662.25
18	COM1	COM17	-2404.75	-779.75
19	COM0	COM16	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	D0(SA0)	2277.25	907.25
88	D1(SA1)	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	NC		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	NC		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM31	COM15	-1028.5	907.25
122	COM30	COM14	-1123.5	907.25
123	COM29	COM13	-1218.5	907.25
124	COM28	COM12	-1313.5	907.25
125	COM27	COM11	-1408.5	907.25
126	COM26	COM10	-1503.5	907.25
127	COM25	COM9	-1598.5	907.25
128	COM24	COM8	-1693.5	907.25
129	COM23	COM7	-1788.5	907.25
130	COM22	COM6	-1924.75	907.25
131	COM21	COM5	-2032.25	907.25
132	COM20	COM4	-2149.75	907.25
133	COM19	COM3	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ PAD CENTER COORDINATES (4-SPI Interface)

DUTY=1/64 duty, SHL=0, SHLA=X

Pad	Pin Name		X	Y
	Master	Slave		
1	COM13	COM45	-2404.75	907.25
2	COM14	COM46	-2404.75	779.75
3	COM15	COM47	-2404.75	662.25
4	COM16	COM48	-2404.75	554.75
5	COM17	COM49	-2404.75	462.75
6	COM18	COM50	-2404.75	370.25
7	COM19	COM51	-2404.75	277.75
8	COM20	COM52	-2404.75	185.25
9	COM21	COM53	-2404.75	92.75
10	COM22	COM54	-2404.75	0.25
11	COM23	COM55	-2404.75	-92.25
12	COM24	COM56	-2404.75	-184.75
13	COM25	COM57	-2404.75	-277.25
14	COM26	COM58	-2404.75	-369.75
15	COM27	COM59	-2404.75	-462.25
16	COM28	COM60	-2404.75	-554.75
17	COM29	COM61	-2404.75	-662.25
18	COM30	COM62	-2404.75	-779.75
19	COM31	COM63	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	NC	2277.25	907.25
88	NC	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	CS1BP		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	A0		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM0	COM32	-1028.5	907.25
122	COM1	COM33	-1123.5	907.25
123	COM2	COM34	-1218.5	907.25
124	COM3	COM35	-1313.5	907.25
125	COM4	COM36	-1408.5	907.25
126	COM5	COM37	-1503.5	907.25
127	COM6	COM38	-1598.5	907.25
128	COM7	COM39	-1693.5	907.25
129	COM8	COM40	-1788.5	907.25
130	COM9	COM41	-1924.75	907.25
131	COM10	COM42	-2032.25	907.25
132	COM11	COM43	-2149.75	907.25
133	COM12	COM44	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ PAD CENTER COORDINATES (4-SPI Interface)

DUTY=1/64 duty, SHL=1, SHLA=0

Pad	Pin Name		X	Y
	Master	Slave		
1	COM50	COM18	-2404.75	907.25
2	COM49	COM17	-2404.75	779.75
3	COM48	COM16	-2404.75	662.25
4	COM47	COM15	-2404.75	554.75
5	COM46	COM14	-2404.75	462.75
6	COM45	COM13	-2404.75	370.25
7	COM44	COM12	-2404.75	277.75
8	COM43	COM11	-2404.75	185.25
9	COM42	COM10	-2404.75	92.75
10	COM41	COM9	-2404.75	0.25
11	COM40	COM8	-2404.75	-92.25
12	COM39	COM7	-2404.75	-184.75
13	COM38	COM6	-2404.75	-277.25
14	COM37	COM5	-2404.75	-369.75
15	COM36	COM4	-2404.75	-462.25
16	COM35	COM3	-2404.75	-554.75
17	COM34	COM2	-2404.75	-662.25
18	COM33	COM1	-2404.75	-779.75
19	COM32	COM0	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	NC	2277.25	907.25
88	NC	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	CS1BP		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	A0		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM63	COM31	-1028.5	907.25
122	COM62	COM30	-1123.5	907.25
123	COM61	COM29	-1218.5	907.25
124	COM60	COM28	-1313.5	907.25
125	COM59	COM27	-1408.5	907.25
126	COM58	COM26	-1503.5	907.25
127	COM57	COM25	-1598.5	907.25
128	COM56	COM24	-1693.5	907.25
129	COM55	COM23	-1788.5	907.25
130	COM54	COM22	-1924.75	907.25
131	COM53	COM21	-2032.25	907.25
132	COM52	COM20	-2149.75	907.25
133	COM51	COM19	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ PAD CENTER COORDINATES (4-SPI Interface)

DUTY=1/64 duty, SHL=1, SHLA=1

Pad	Pin Name		X	Y
	Master	Slave		
1	COM18	COM50	-2404.75	907.25
2	COM17	COM49	-2404.75	779.75
3	COM16	COM48	-2404.75	662.25
4	COM15	COM47	-2404.75	554.75
5	COM14	COM46	-2404.75	462.75
6	COM13	COM45	-2404.75	370.25
7	COM12	COM44	-2404.75	277.75
8	COM11	COM43	-2404.75	185.25
9	COM10	COM42	-2404.75	92.75
10	COM9	COM41	-2404.75	0.25
11	COM8	COM40	-2404.75	-92.25
12	COM7	COM39	-2404.75	-184.75
13	COM6	COM38	-2404.75	-277.25
14	COM5	COM37	-2404.75	-369.75
15	COM4	COM36	-2404.75	-462.25
16	COM3	COM35	-2404.75	-554.75
17	COM2	COM34	-2404.75	-662.25
18	COM1	COM33	-2404.75	-779.75
19	COM0	COM32	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	NC	2277.25	907.25
88	NC	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	CS1BP		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	A0		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM31	COM63	-1028.5	907.25
122	COM30	COM62	-1123.5	907.25
123	COM29	COM61	-1218.5	907.25
124	COM28	COM60	-1313.5	907.25
125	COM27	COM59	-1408.5	907.25
126	COM26	COM58	-1503.5	907.25
127	COM25	COM57	-1598.5	907.25
128	COM24	COM56	-1693.5	907.25
129	COM23	COM55	-1788.5	907.25
130	COM22	COM54	-1924.75	907.25
131	COM21	COM53	-2032.25	907.25
132	COM20	COM52	-2149.75	907.25
133	COM19	COM51	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ PAD CENTER COORDINATES (4-SPI Interface)

DUTY=1/32 duty, SHL=0, SHLA=X

Pad	Pin Name		X	Y
	Master	Slave		
1	COM13	COM29	-2404.75	907.25
2	COM14	COM30	-2404.75	779.75
3	COM15	COM31	-2404.75	662.25
4	COM16	COM0	-2404.75	554.75
5	COM17	COM1	-2404.75	462.75
6	COM18	COM2	-2404.75	370.25
7	COM19	COM3	-2404.75	277.75
8	COM20	COM4	-2404.75	185.25
9	COM21	COM5	-2404.75	92.75
10	COM22	COM6	-2404.75	0.25
11	COM23	COM7	-2404.75	-92.25
12	COM24	COM8	-2404.75	-184.75
13	COM25	COM9	-2404.75	-277.25
14	COM26	COM10	-2404.75	-369.75
15	COM27	COM11	-2404.75	-462.25
16	COM28	COM12	-2404.75	-554.75
17	COM29	COM13	-2404.75	-662.25
18	COM30	COM14	-2404.75	-779.75
19	COM31	COM15	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	NC	2277.25	907.25
88	NC	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	CS1BP		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	A0		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM0	COM16	-1028.5	907.25
122	COM1	COM17	-1123.5	907.25
123	COM2	COM18	-1218.5	907.25
124	COM3	COM19	-1313.5	907.25
125	COM4	COM20	-1408.5	907.25
126	COM5	COM21	-1503.5	907.25
127	COM6	COM22	-1598.5	907.25
128	COM7	COM23	-1693.5	907.25
129	COM8	COM24	-1788.5	907.25
130	COM9	COM25	-1924.75	907.25
131	COM10	COM26	-2032.25	907.25
132	COM11	COM27	-2149.75	907.25
133	COM12	COM28	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ PAD CENTER COORDINATES (4-SPI Interface)

DUTY=1/32 duty, SHL=1, SHLA=X

Pad	Pin Name		X	Y
	Master	Slave		
1	COM18	COM2	-2404.75	907.25
2	COM17	COM1	-2404.75	779.75
3	COM16	COM0	-2404.75	662.25
4	COM15	COM31	-2404.75	554.75
5	COM14	COM30	-2404.75	462.75
6	COM13	COM29	-2404.75	370.25
7	COM12	COM28	-2404.75	277.75
8	COM11	COM27	-2404.75	185.25
9	COM10	COM26	-2404.75	92.75
10	COM9	COM25	-2404.75	0.25
11	COM8	COM24	-2404.75	-92.25
12	COM7	COM23	-2404.75	-184.75
13	COM6	COM22	-2404.75	-277.25
14	COM5	COM21	-2404.75	-369.75
15	COM4	COM20	-2404.75	-462.25
16	COM3	COM19	-2404.75	-554.75
17	COM2	COM18	-2404.75	-662.25
18	COM1	COM17	-2404.75	-779.75
19	COM0	COM16	-2404.75	-907.25
20	SEG63		-2277.25	-907.25
21	SEG62		-2149.75	-907.25
22	SEG61		-2032.25	-907.25
23	SEG60		-1924.75	-907.25
24	SEG59		-1832.25	-907.25
25	SEG58		-1739.75	-907.25
26	SEG57		-1647.25	-907.25
27	SEG56		-1554.75	-907.25
28	SEG55		-1462.25	-907.25
29	SEG54		-1369.75	-907.25
30	SEG53		-1277.25	-907.25
31	SEG52		-1184.75	-907.25
32	SEG51		-1092.25	-907.25
33	SEG50		-999.75	-907.25
34	SEG49		-907.25	-907.25
35	SEG48		-814.75	-907.25
36	SEG47		-722.25	-907.25
37	SEG46		-629.75	-907.25
38	SEG45		-537.25	-907.25
39	SEG44		-444.75	-907.25
40	SEG43		-352.25	-907.25
41	SEG42		-259.75	-907.25
42	SEG41		-167.25	-907.25
43	SEG40		-74.75	-907.25
44	SEG39		17.75	-907.25

Pad No.	Pin Name	X	Y
45	SEG38	110.25	-907.25
46	SEG37	202.75	-907.25
47	SEG36	295.25	-907.25
48	SEG35	387.75	-907.25
49	SEG34	480.25	-907.25
50	SEG33	572.75	-907.25
51	SEG32	665.25	-907.25
52	SEG31	757.75	-907.25
53	SEG30	850.25	-907.25
54	SEG29	942.75	-907.25
55	SEG28	1035.25	-907.25
56	SEG27	1127.75	-907.25
57	SEG26	1220.25	-907.25
58	SEG25	1312.75	-907.25
59	SEG24	1405.25	-907.25
60	SEG23	1497.75	-907.25
61	SEG22	1590.25	-907.25
62	SEG21	1682.75	-907.25
63	SEG20	1775.25	-907.25
64	SEG19	1867.75	-907.25
65	SEG18	1960.25	-907.25
66	SEG17	2052.25	-907.25
67	SEG16	2159.75	-907.25
68	SEG15	2277.25	-907.25
69	SEG14	2404.75	-907.25
70	SEG13	2404.75	-779.75
71	SEG12	2404.75	-652.25
72	SEG11	2404.75	-534.75
73	SEG10	2404.75	-427.25
74	SEG9	2404.75	-334.75
75	SEG8	2404.75	-242.25
76	SEG7	2404.75	-149.75
77	SEG6	2404.75	-57.25
78	SEG5	2404.75	35.25
79	SEG4	2404.75	127.75
80	SEG3	2404.75	220.25
81	SEG2	2404.75	312.75
82	SEG1	2404.75	405.25
83	SEG0	2404.75	512.75
84	ADCP	2404.75	630.25
85	CLL	2404.75	757.75
86	VSS	2404.75	907.25
87	NC	2277.25	907.25
88	NC	2159.75	907.25

Pad No.	Pin Name		X	Y
	Master	Slave		
89	NC		2052.25	907.25
90	NC		1916.5	907.25
91	NC		1821.5	907.25
92	NC		1726.5	907.25
93	D6(SDA)		1631.5	907.25
94	D7(SCLK)		1536.5	907.25
95	CS1BP		1441.5	907.25
96	NC		1346.5	907.25
97	NC		1251.5	907.25
98	A0		1156.5	907.25
99	NC		1061.5	907.25
100	VDD		966.5	907.25
101	RSTP		871.5	907.25
102	CLSP		776.5	907.25
103	FRR		681.5	907.25
104	MSP		586.5	907.25
105	BS1P		491.5	907.25
106	BS0P		396.5	907.25
107	SHLP		301.5	907.25
108	VDD2		206.5	907.25
109	CAP2N		111.5	907.25
110	CAP2P		16.5	907.25
111	CAP1P		-78.5	907.25
112	CAP1N		-173.5	907.25
113	CAP3P		-268.5	907.25
114	VOUT		-363.5	907.25
115	V0		-458.5	907.25
116	VRAB		-553.5	907.25
117	V3		-648.5	907.25
118	V2		-743.5	907.25
119	V4		-838.5	907.25
120	V1		-933.5	907.25
121	COM31	COM15	-1028.5	907.25
122	COM30	COM14	-1123.5	907.25
123	COM29	COM13	-1218.5	907.25
124	COM28	COM12	-1313.5	907.25
125	COM27	COM11	-1408.5	907.25
126	COM26	COM10	-1503.5	907.25
127	COM25	COM9	-1598.5	907.25
128	COM24	COM8	-1693.5	907.25
129	COM23	COM7	-1788.5	907.25
130	COM22	COM6	-1924.75	907.25
131	COM21	COM5	-2032.25	907.25
132	COM20	COM4	-2149.75	907.25
133	COM19	COM3	-2277.25	907.25

134	Test2	2292.3	757.75

135	Test1	966.5	774.75

■ Pin Description

(1)Power Pins

Name	I/O	Description
VDD	-	Connected to the +5V 0r +3V dc power. Common to the Vcc MPU power pin.
VDD2		This is the reference power supply for the Step-up voltage circuit.
VSS	-	0V dc pin connected to the system ground.
CAP1P~3P CAP1N~2N	-	Capacitor connector pin for voltage booster.
V0~V4	-	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: V0 ≧ V1 ≧ V2 ≧ V3 ≧V4 ≧ VSS

(2)System Bus Connection Pins

IIC Interface

Name	I/O	Description
D7(SCLK) D6(SDA) D1(SA1) D0(SA0)	I/O	SCLK: serial interface clock input SDA : serial data input SA0、SA1:slave address
Test1	**I**	**Test1 Pin must be bonding to PCB Size VDD**
Test2	**I**	**Floating**

4-SPI Interface

Name	I/O	Description
D7(SCLK) D6(SDA)	I/O	SCLK: serial interface clock input SDA : serial data input
A0	I	Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0: display control data. A0=1: display data.
CS1BP	I	Input. When CS1BP = 0 the chip select become active
Test1	**I**	**Test1 Pin must be bonding to PCB Size VDD**
Test2	**I**	**Test2 Pin must be bonding to PCB Size VSS**

Name	I/O	Description
CLS	I	CLS=1 : internal oscillator enable CLS=0 : external clock operation mode
ADCP	I	The pin selects the relationship between display data RAM column addresses and segment drivers. **ADCP=1: SEG0←column address 3FH,…..inverted** **ADCP=0: SEG0←column address 00H,…..normal**
SHLP	I	The pin selects the com output scan direction. **SHL=1: Reverse direction,com63→com0** **SHL=0: Normal com0→com63** **Both master and slave should set identical SHL value**
BS1P,BS0P	I	Select LCD Bias 1/5, 1/6, 1/8, 1/9 bias **BS1P=0, BS0P=0 : 1/5 bias** **BS1P=0, BS0P=1 : 1/6 bias** **BS1P=1, BS0P=0 : 1/8 bias** **BS1P=1, BS0P=1 : 1/9 bias**
$\overline{\text{RST}}$	I	Input low active. System reset.

(3)LCD Driver Circuit Signals

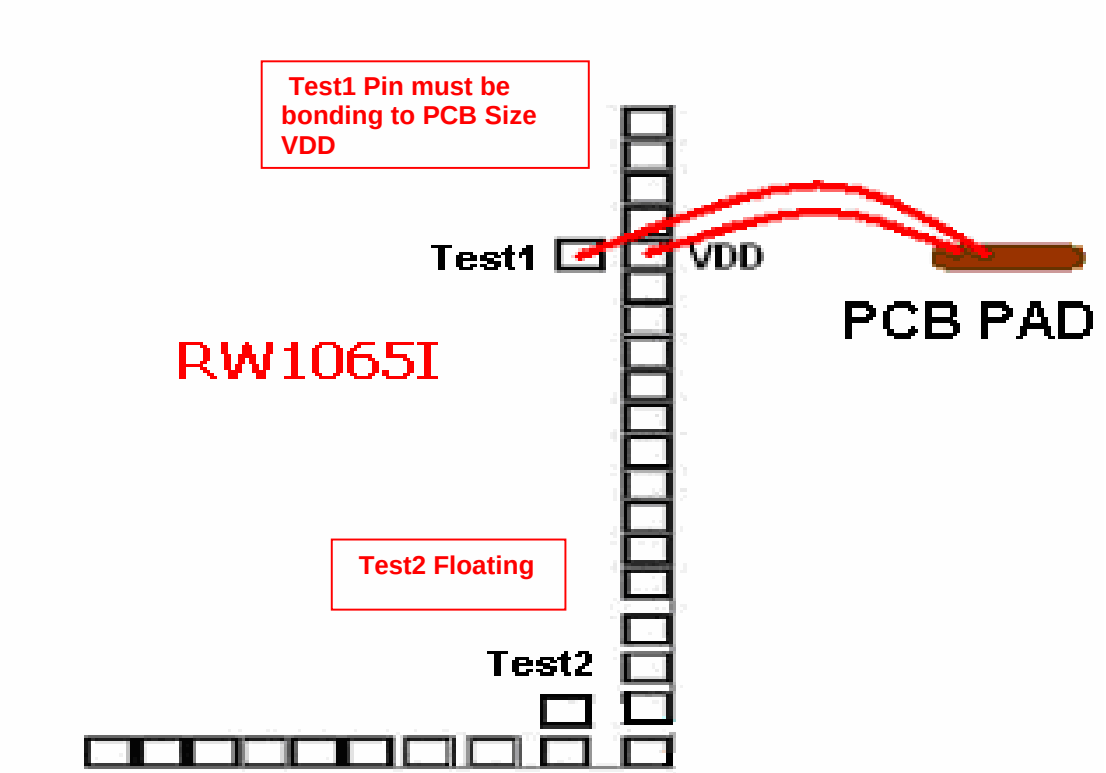
<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>CLL</td><td>I/O</td><td>Input/output.
I/O selection
● M/S = “H” & CLS = “H” ：Output
● M/S = “L” & CLS = “H” ：Input
● M/S = “X” & CLS = “L” ：Input

This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges.</td></tr>
<tr><td>SEGn</td><td>O</td><td>Output.
A single level of V0, V2, V3 and VSS is selected by the combination of display RAM contents and FR signal.</td></tr>
<tr><td>COMn</td><td>O</td><td>Output.
The output pin for LCD common (row) driving. A single level of V0, V1, V4 and VSS is selected by the combination of common counter output and FR signal. The slave LSI has the reverse common output scan sequence than the master LSI.</td></tr>
<tr><td>FRR</td><td>I/O</td><td>Input/output.
This is the liquid crystal alternating current signal I/O terminal
I/O selection
● M/S = “H”：Output
● M/S = “L”：Input</td></tr>
<tr><td>VRAB</td><td>I</td><td>Provides the voltage between V0 and VSS through a resistive voltage divider.</td></tr>
<tr><td>M/S</td><td>I</td><td>Input.
The master or slave LSI operation select pin for the RW1065I.

<table>
<tr><th>M/S</th><th>Operating Mode</th><th>FR</th><th>CL</th><th>V0~V4</th><th>Power Supply</th><th>Internal OSC</th><th>COMMON Output</th><th>SEG output</th></tr>
<tr><td>High</td><td>Master</td><td>Output</td><td>See CLS</td><td>On</td><td>On</td><td>See CLS</td><td>COM0-31</td><td>SEG0-63</td></tr>
<tr><td>Low</td><td>Slave</td><td>Input</td><td>Input</td><td>Off</td><td>Off</td><td>Off</td><td>COM32-63</td><td>SEG64-127</td></tr>
</table>
</td></tr>
</table>

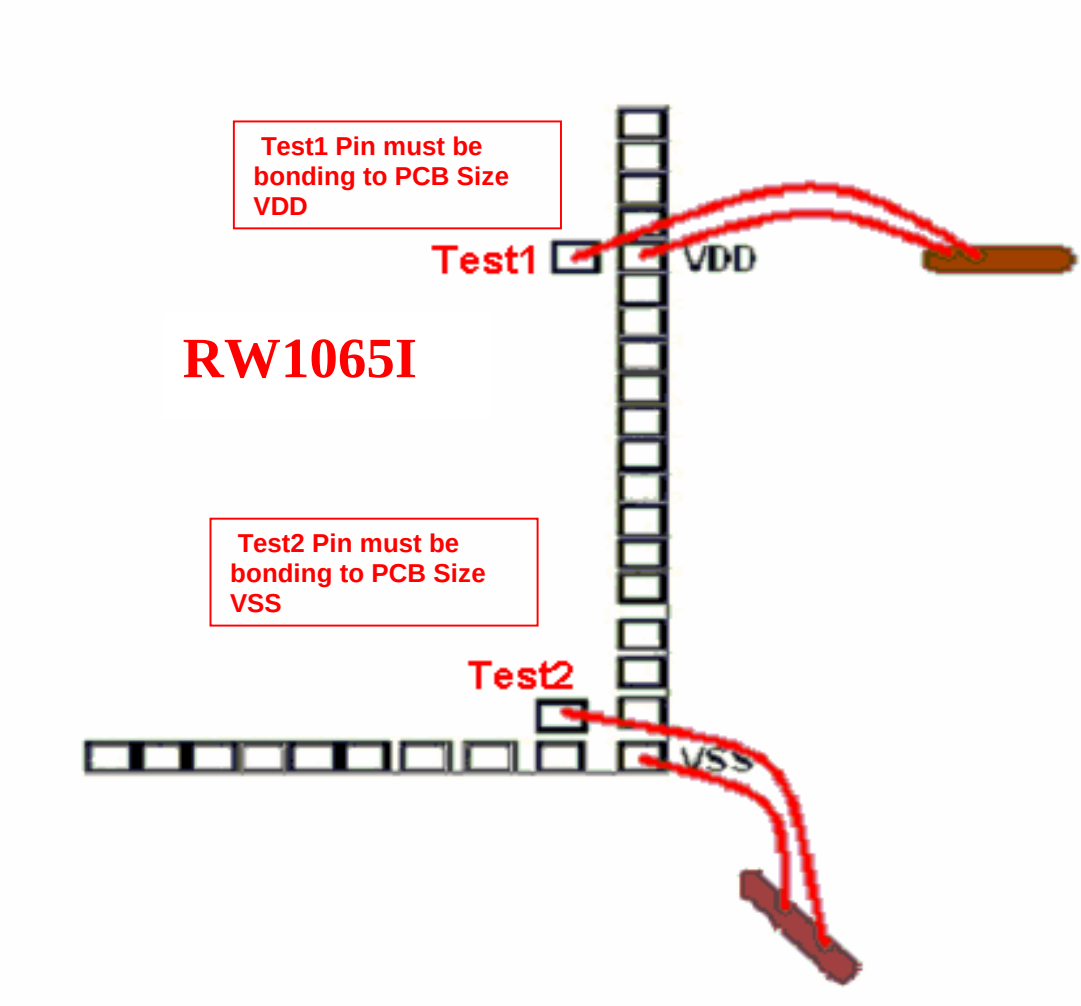
■ Bonding Description

IIC Interface bonding setting



■ Bonding Description

4-SPI Interface bonding setting



➢ IIC Interface

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line SDA (DB6) and a Serial Clock line SCLK (DB7). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.
* When IIC interface is selected, the INF register must be set to “1”.

◆ BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.2.1

◆ START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.2.2

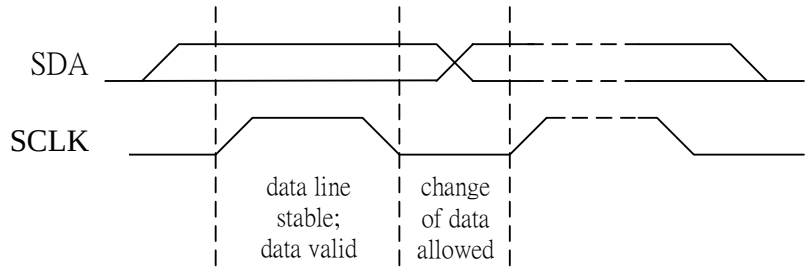


Fig 2.1 Bit transfer

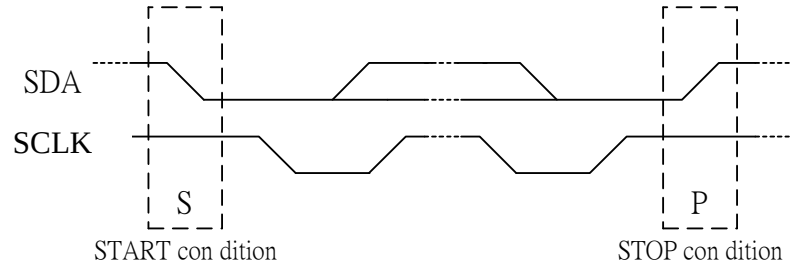


Fig 2.2 Definition of START and STOP conditions

◆ SYSTEM CONFIGURATION

The system configuration is illustrated in Fig2.3

· Transmitter: the device, which sends the data to the bus
· Receiver: the device, which receives the data from the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

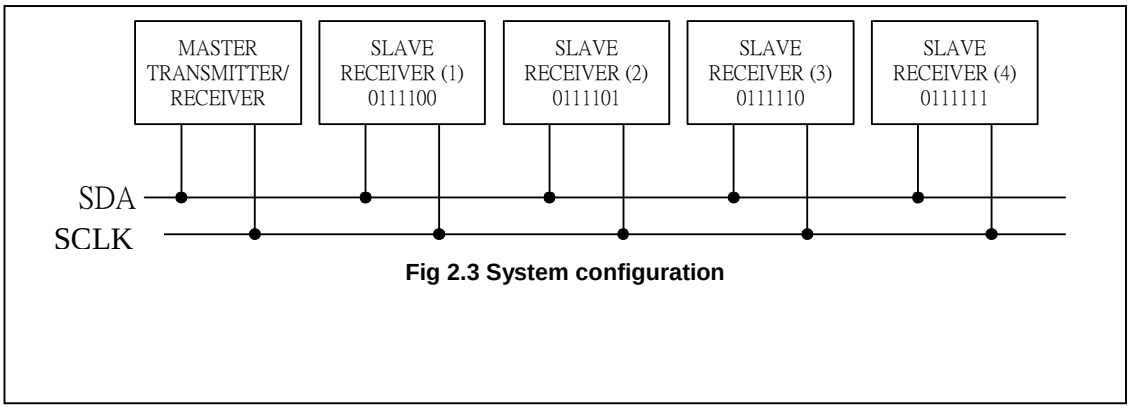


Fig 2.3 System configuration

◆ ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Fig.2.4

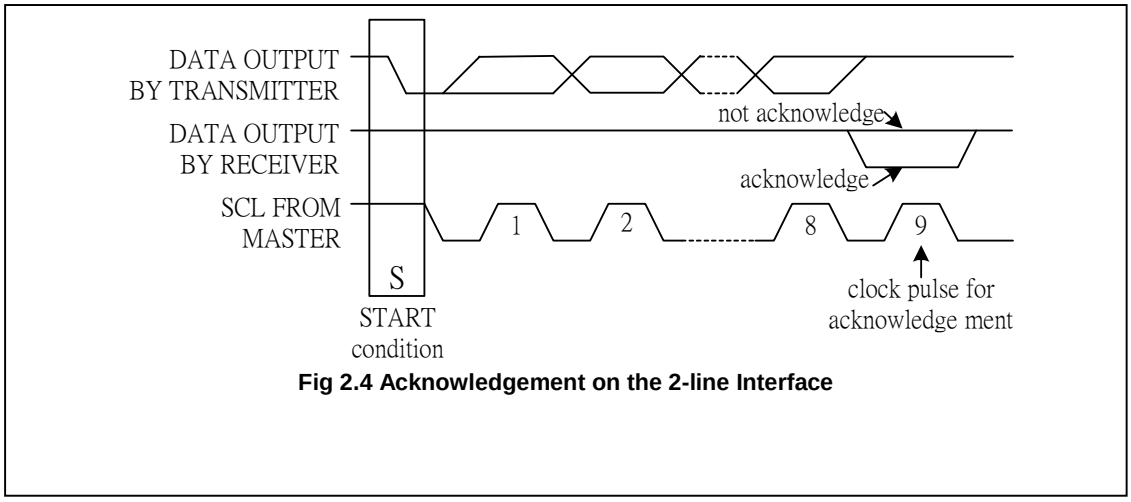


Fig 2.4 Acknowledgement on the 2-line Interface

◆ IIC Interface protocol

The RW1065**I** supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the RW1065**I**. The least significant bit of the slave address is set by connecting the input SA0 (D0) and SA1 (D1) to either logic 0 (or logic 1 (VDD)).
The IIC Interface protocol is illustrated in Fig.2.5

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended RW1065**I** device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

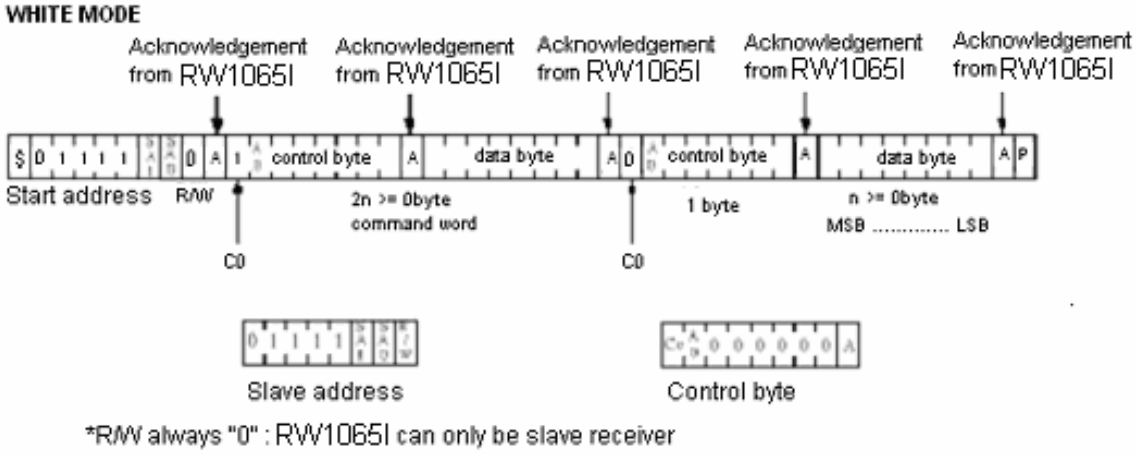


Fig .2.5 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

➢ 4-SPI serial interface

If 4-Pin SPI mode is used, CS1B, SCLK (DB7), SDA (DB6), and A0 (RS) are used. They are chip selection; serial clock input, serial data input, and data/instruction section, relatively. The example of timing sequence is shown below Figure 1.

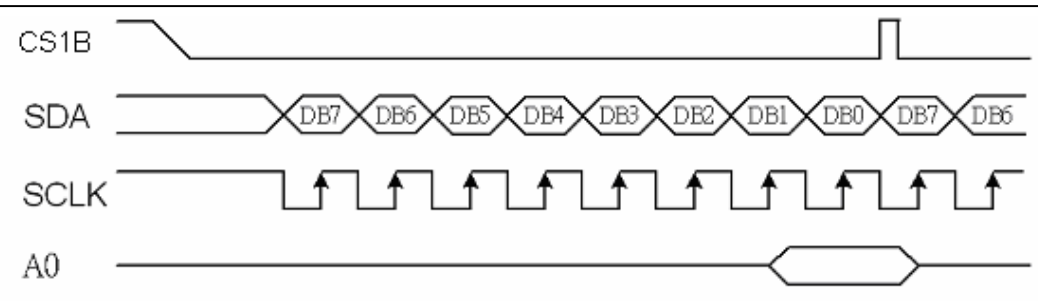


Figure1 4-line SPI Timing

The Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (tCYC) requirement alone in accessing the RW1065**I** Series. Wait time may not be considered.
And, in the RW1065**I** Series chips, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. Internal data bus.
For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle. There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.

Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 64 (8 page x 8 bit) x 64 bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display data transfer when multiple RW1065**I** series chips are used, thus and display structures can be created easily and with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

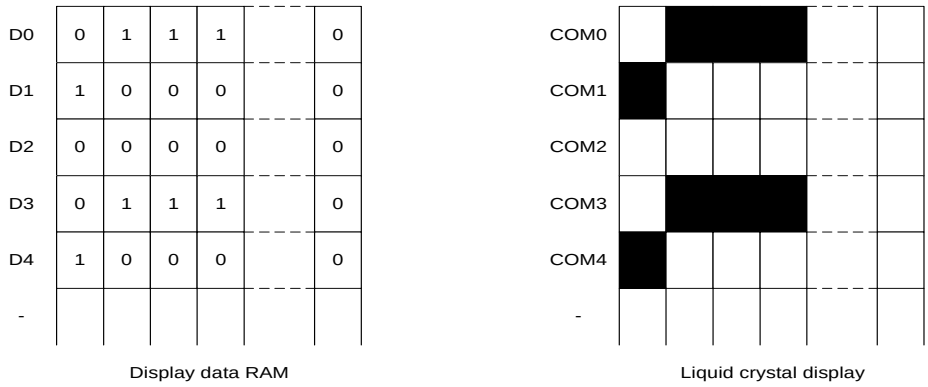


Figure 3

The Page Address Circuit

As shown in Figure 4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

The Column Address

As is shown in Table 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the increment of column addresses stops with 3FH. Because the column address is independent of the page address, when moving, for example, from page 0 column 3FH to page 1 column 00H, it is necessary to re-specify both the page address and the column address.

Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output / ADC set	SEG0		SEG 63
ADC(D0)=0	0	→ Column Address →	63
ADC(D0)=1	63	← Column Address ←	0

Page Address				Data	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	.....	SEG55	SEG56	SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63	SEG / COM
D3	D2	D1	D0																					
0	0	0	0	D0	■	■	■	■	■					Page 0										COM0
				D1			■																	COM1
				D2			■																	COM2
				D3			■																	COM3
				D4			■																	COM4
				D5			■																	COM5
				D6			■																	COM6
				D7																				COM7
0	0	0	1	D0	■	■	■	■	■					Page 1										COM8
				D1	■																			COM9
				D2	■																			COM10
				D3	■	■	■	■																COM11
				D4	■																			COM12
				D5	■																			COM13
				D6	■	■	■	■	■															COM14
				D7																				COM15
0	0	1	0	D0		■	■	■						Page 2										COM16
				D1	■				■															COM17
				D2	■																			COM18
				D3		■	■	■																COM19
				D4					■															COM20
				D5	■				■															COM21
				D6		■	■	■																COM22
				D7																				COM23
0	0	1	1	D0	■	■	■	■	■					Page 3										COM24
				D1			■																	COM25
				D2			■																	COM26
				D3			■																	COM27
				D4			■																	COM28
				D5			■																	COM29
				D6			■																	COM30
				D7																				COM31
COLUMN				ADC=0	00	01	02	03	04	05	06	07	08	.....	55	56	57	58	59	60	61	62	63	
				ADC=1	63	62	61	60	59	58	57	56	55	.....	08	07	06	05	04	03	02	01	00	

Figure 4

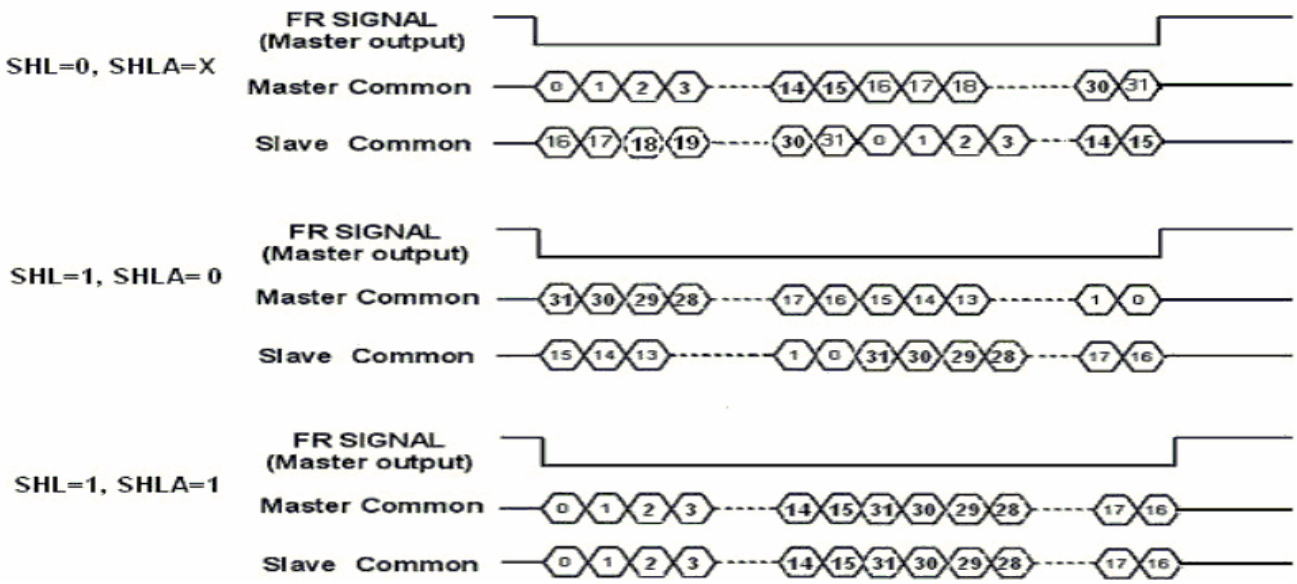
- **Common Timing Generator Circuit**

Generates common timing signals and FR frame signals from the CL basic clock. The 1/32 or 1/64 duty (for RW1065I) can be selected by the Duty Select command. The 1/32 and 1/64 duties are provided by two chips consisting of the master and slave chips in the common multi-chip mode.

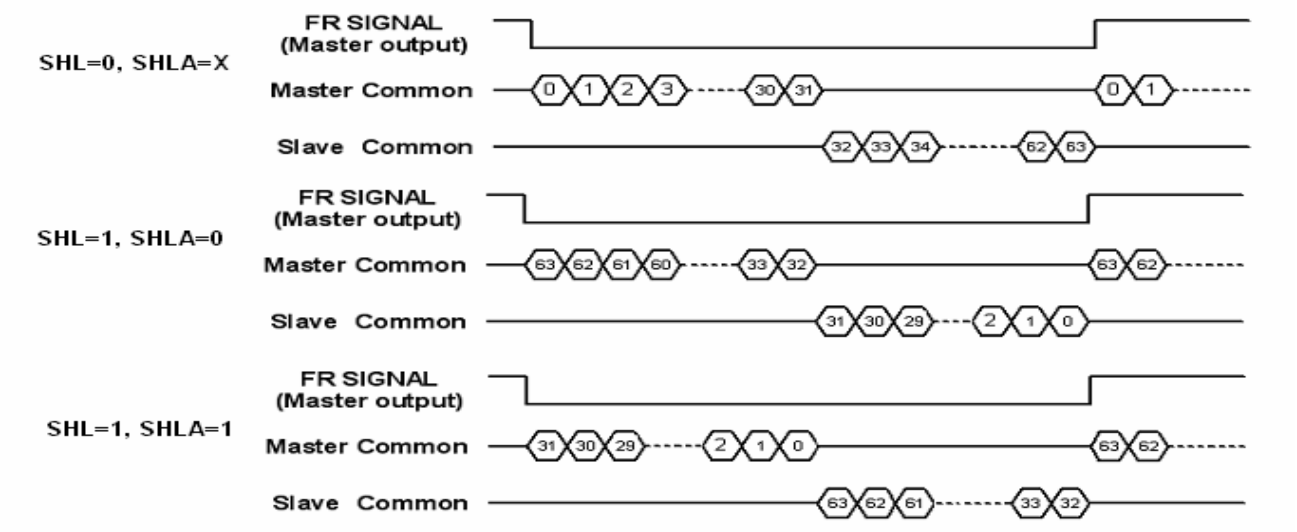
- **Display Data Latch Circuit**

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF.

➢ **1/32 duty:**



➢ **1/64 duty:**



Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

➢ Two-frame alternating current drive waveform

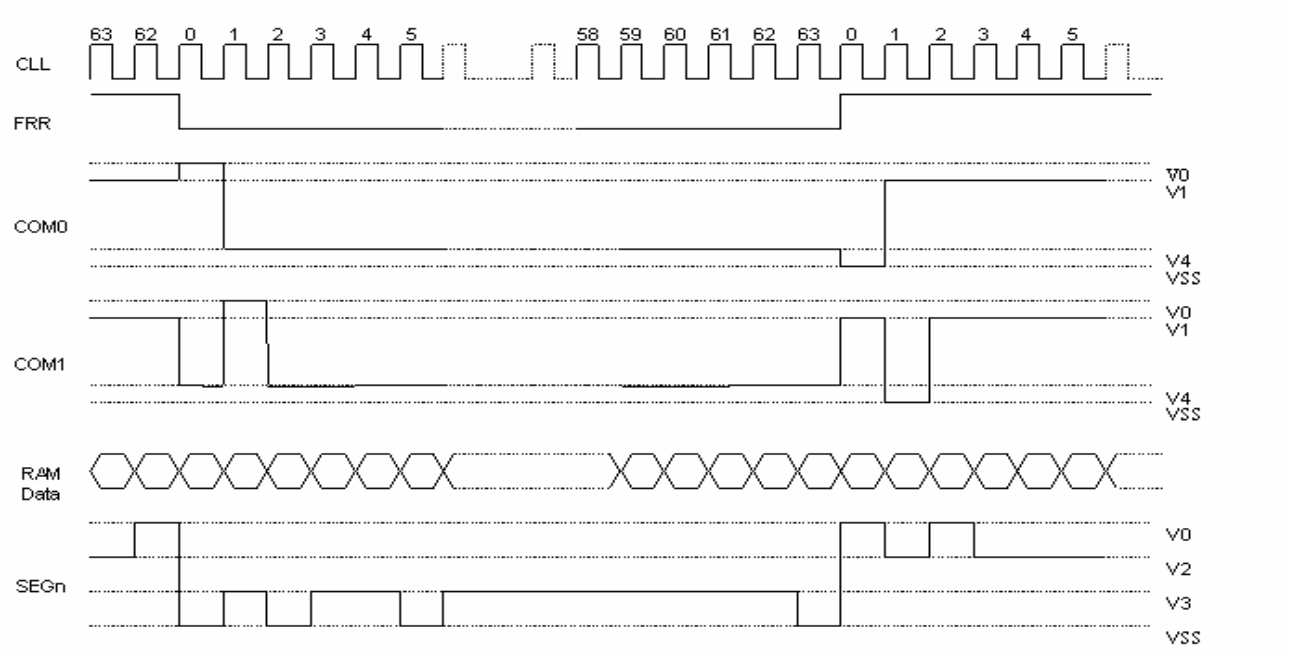


Figure 5

When multiple RW1065I Series chips are used, the slave chip must be supplied the display timing signals (FR, CL) from the master chip.

Table 5 shows the status of the FR and CL signals.

Table 5

Operating Mode		FR	CL
Master (M/S = "H")	The internal oscillator circuit is enabled (CLS = "H")	Output	Output
	The internal oscillator circuit is disabled (CLS = "L")	Output	Input
Slave (M/S = "L")	The internal oscillator circuit is enabled (CLS = "H")	Input	Input
	The internal oscillator circuit is disabled (CLS = "L")	Input	Input

The Liquid Crystal Driver Circuits

These are a 64-channel (RW1065**I**) that generates four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal and the FR signal produces the liquid crystal drive voltage output. Figure 6 shows examples of the SEG and COM output waveform.

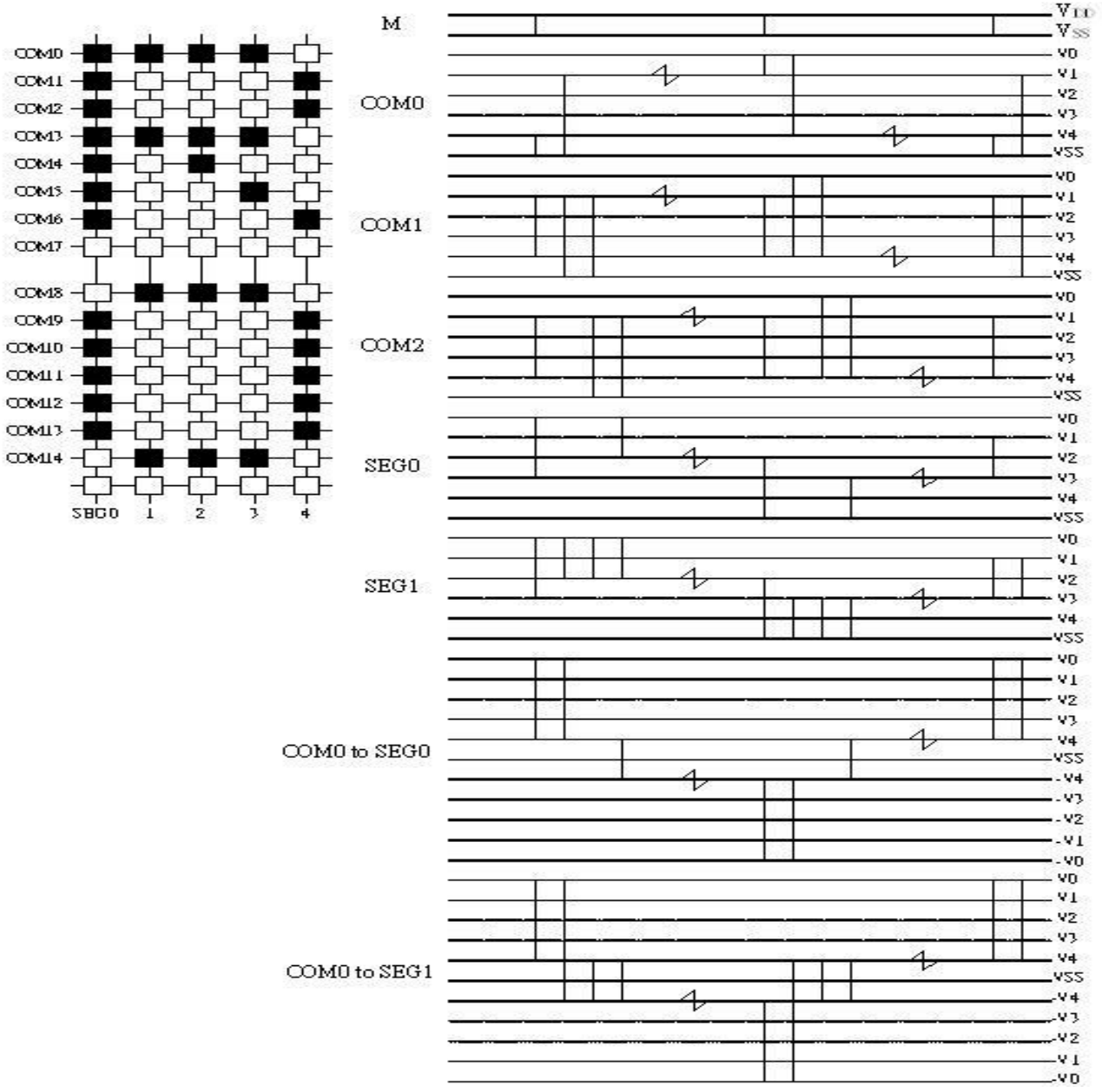


Figure 6

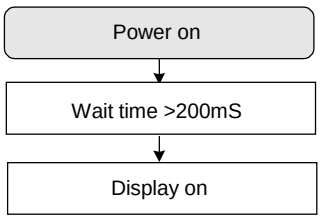
The Power Supply Circuit

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, and voltage follower circuits. **They are only enabled in master operation.**
The power supply circuits can turn on automatically after power on.

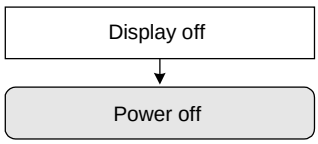
Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel.

The Liquid Crystal Voltage Generator Circuit

The V0 voltage is produced by a resistive voltage divider outside the IC through VRAB pin, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3 and V4 to the liquid crystal drive circuit.
1/5 bias or 1/6 bias or 1/8 bias or 1/9 bias for RW1065I, can be selected by BS0 and BS1 pins.
V0-Vss maximum voltage is 15V, Vout-Vss maximum voltage is 17V.
If VDD < 3.5V , it can use the Booster circuit 2x,3x,4x,The booster voltage can follow the spec. condition (Vout-Vss ≦ 17V max. voltage.) if VDD >3.5V only use the 2X,3X, booster circuit, that can ensure the V0-Vss voltage ≦ 15V. If use the VDD voltage 5V and 4X booster, it's over the spec. operation condition.
To turn on built-in power (booster/follower) must waiting 200mS to display on for booster/follower stable. Therefore, power off must follower "power off sequence" too.



Power on sequence



Power off sequence

The Reset Circuit

When the RTP input comes to the “L” level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF
2. Display all point on is select to normal
3. Display normal/reverse is select to normal
4. 1/64 duty is selected
5. Read modify write OFF
6. Column address set to Address 0
7. Page address set to Page 0
8. Start line set to first line
9. Frame frequency set to default
10. Power save mode released
11. Ext set to “0”

When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the RSTP terminal. After the initialization, each input terminal should be controlled normally.
While RSTP is “L,” the oscillator works but the display timing generator stops, and the CL, FR, terminals are fixed to “H.” The terminals D0 to D7 are not affected.

■ TABLE OF RW1065I INSTRUCTIONS

Instruction		Instruction code								Description
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
EXT=0 or 1										
MODE SET		0	0	0	0	1	1	0	EXT	Set EXT mode

Instruction		Instruction code								Description
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
EXT=0										
Display ON/OFF		0	0	1	1	1	1	1	D	D=0:Display OFF D=1:Display ON
Set page address		1	0	1	1	1	P2	P1	P0	Set page address
Set column address		0	1	Y5	Y4	Y3	Y2	Y1	Y0	Set column address MSB
Read Status		BUSY	0	ON /OFF	RESET	0	0	0	0	Read register status
Write display data		Write data								Write data into DDRAM
Set initial display line register		1	1	S5	S4	S3	S2	S1	S0	Specify the initial display line to realize vertical scrolling

Instruction		Instruction code								Description
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
EXT=1										
NOP		0	0	0	0	0	0	0	0	no operation
Common output scan (double command)		0	0	0	0	0	1	1	0	Extra option command for common output
		0	0	0	0	0	0	0	SHLA	
Set power save mode		0	0	0	0	0	0	1	PSAVE	P=0: normal mode P=1: sleep mode
Display COMMAND (double command)		0	0	0	0	0	1	0	1	**DUTY=1: 64 duty** **DUTY=0: 32 duty** **ALLON=1:display all on** **ALLON=0:display normal** **REV=1:display reverse** **REV=0:display normal** **FRSEL=1:FR frequency double default** **FRSEL=0:FR frequency default**
		FRSEL	0	0	0	0	REV	ALL ON	DUTY	

■ Command Description

See the Table of RW1065**I** instructions. The RW1065**I** series identifies a data bus using a combination of RS, E and RW signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

➢ Display ON/OFF

EXT	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	1	1	D

This command turns the display on and off.
D=1: Display ON
D=0: Display OFF(default)

➢ Set page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified.
The display status is not changed even when the page address is changed.

EXT	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	A2	A1	A0

- This command loads the page address register.

A2	A1	A0	Page
0	0	0	0 (default)
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Page mapping see Figure 4

➢ Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by I each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 63, and the page address is not changed continuously.

EXT	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0(default)
0	0	0	0	0	1	1
			.			.
			.			.
			.			.
			.			.
1	1	1	1	1	1	63

➢ Write Display Data

EXT	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page, address registers and then increments the column address register by one.

➢ Set initial display line register

EXT	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	S5	S4	S3	S2	S1	S0

Loads the RAM line address of the initial display line, COM 0, into the initial display line register. The RAM display data becomes the top line of the LCD screen. It is followed by the higher number lines in ascending order, corresponding to the duty cycle. The screen can be scrolled using this command by incrementing the line address.(default value=”00H”)

➢ Set power save mode

EXT	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0	1	PSAVE

When power save mode is entered, thus greatly reducing power consumption.
In the power save mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.

PSAVE=1: Sleep mode
PSAVE=0: Normal mode

Sleep mode
This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment and common drive outputs output a V_{SS} level.

➢ Display command :double command

EXT	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	1	0	1
1	0	0	FRSEL	0	0	0	0	REV	ALLON	DUTY

Display Normal/Reverse set
REV=1: Reverse
REV=0: Normal(default)

Display All Point ON/OFF
ALLON=1: All display points ON
ALLON=0: Normal(default)

Select Duty
Duty=1: 1/64 duty cycle(default)
Duty=0: 1/32 duty cycle

FRAME FREQUENCY Select
FRSEL=1: Double
FRSEL=0: (default)

➢ Common output option command :double command

EXT	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	1	1	0
			0	0	0	0	0	0	0	SHLA

This command can be used with Pin SHL to get different output direction of common scan output

➢ Hardware Pin Set

● Select ADC by ADC Pin

The pin selects the relationship between display data RAM column addresses and segment drivers.
ADC=1: SEG0←column address 3FH,…..inverted
ADC=0: SEG0←column address 00H,…..normal(default)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit Board design .See Figure 4 for a table of segments and column addresses for the two values of D.

● Select SHL by SHL Pin

The pin selects the com output scan direction.
SHL=1: Reverse direction,com63→com0
SHL=0: Normal com0→com63

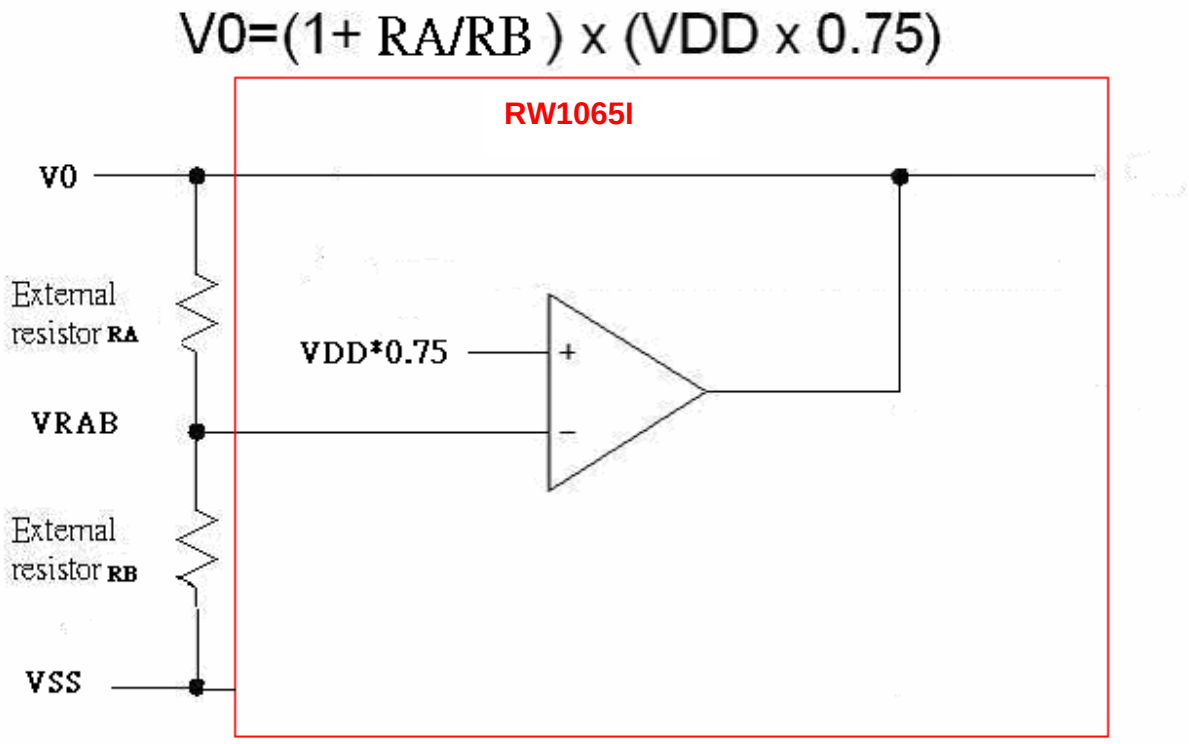
This pin can use with the SHLA software command to get different options of Common output
Please refer to P.6 ~ P.10 to see the details

● Select LCD Bias by BS0, BS1 Pin

BS1	BS0	Bias
0	0	1/5 bias
0	1	1/6 bias
1	0	1/8 bias
1	1	1/9 bias

When an External Resistance is Used

The liquid crystal power supply voltage V_0 is set by adding resistors Ra' and Rb' between V_{DD} and V_R, and between V_R and V_0, respectively.



Notes: a regulated VDD is required for stable V0 value

■ The set voltage circuits

Using the step-up voltage circuits equipped within the RW1065I chips, it is possible to produce a 2X, 3X, 4X, step-up voltage levels.

2X step-up

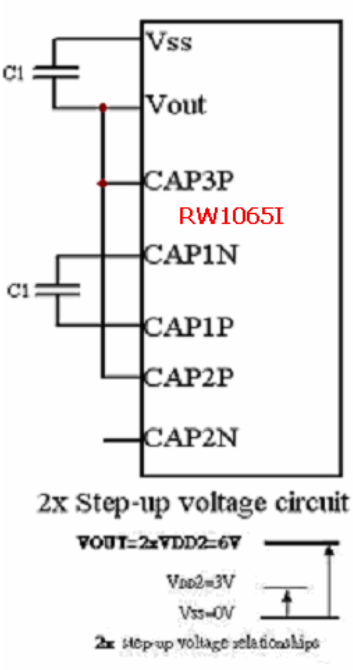
To produce voltage level in the positive direction at the Vout terminal that is 2 times the voltage difference between VSS and VDD2. Please configure set voltage circuits like this.
Place a 1uF~2.2uF capacitor between CAP1N and CAP1P.
Place a 1uF~2.2uF capacitor between VSS and VOUT.
Short CAP2P, CAP3P and VOUT.
Leave CAP2N open.

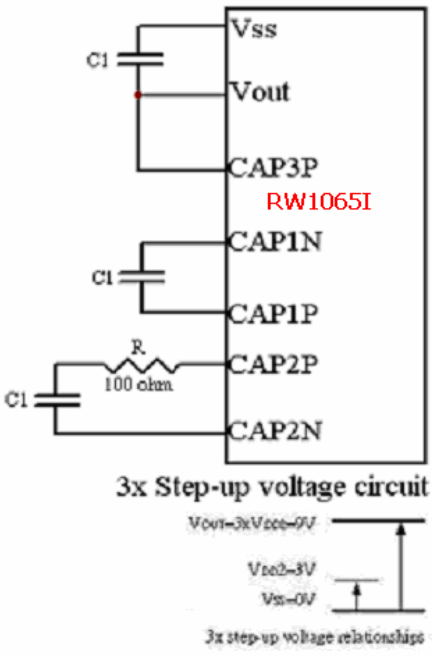
3X step-up

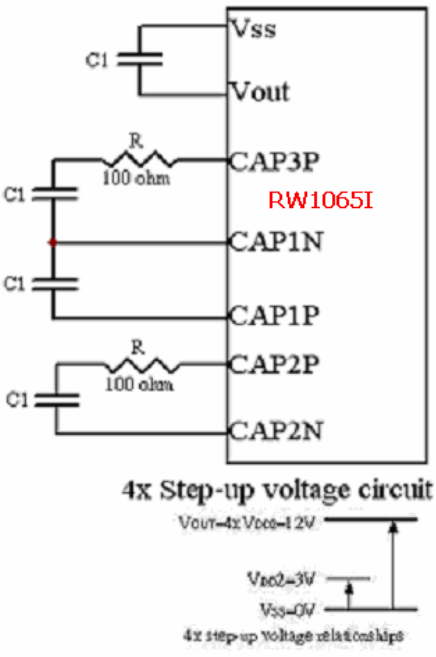
To produce voltage level in the positive direction at the Vout terminal that is 3 times the voltage difference between VSS and VDD2. Please configure set voltage circuits like this.
Place a 1uF~2.2uF capacitor between CAP1N and CAP1P.
Place a 1uF~2.2uF capacitor between VSS and VOUT.
Place a 1uF~2.2uF capacitor and 100 ohms resistor between CAP2N and CAP2P.
Short CAP3P and Vout.

4X step-up

To produce voltage level in the positive direction at the Vout terminal that is 4 times the voltage difference between VSS and VDD2. Please configure set voltage circuits like this.
Place a 1uF~2.2uF capacitor between CAP1N and CAP1P.
Place a 1uF~2.2uF capacitor between VSS and VOUT.
Place a 1uF~2.2uF capacitor and 100 ohms resistor between CAP2N and CAP2P.
Place a 1uF~2.2uF capacitor and 100 ohms resistor between CAP1N and CAP3P.







■ ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power supply voltage	V_{DD}	-0.3 to +7.0	V
LCD driver voltage	Vout	0 to +17	V
Input voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating temperature	T_A	-40 to +85	℃
Storage temperature	T_{STO}	-55 to +125	℃

■ DC CHARACTERISTICS

Unless otherwise specified, Vss=0V, VDD=3.0V

Item		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Operating Voltage		VDD	-		2.7	3.0	5.5	V	V_{DD}*1
Step up output voltage		Vout	(Relative to V_{DD})		0	-	17	V	Vout
Voltage follower circuit operating Voltage		V0	(Relative to V_{DD})		0	-	15	V	V0
V0 accuracy		V0	-		0	-	15	%	V0
High-level Input Voltage Low-level Input Voltage		V_{IHC} V_{ILC}	-		0.7 V_{DD} Vss	-	V_{DD} 0.9	V	*2
High-level Output Voltage Low-level Output Voltage		V_{OHC} V_{OLC}	I_{OH} = –0.5 mA I_{OL} = 0.5 mA		0.8V_{DD} Vss	-	V_{DD} 0.2 V_{DD}	V	*3
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		-1	-	2	uA	*4
Output leakage current		I_{LO}	-		-1		1	uA	*5
Liquid Crystal Driver ON Resistance		R_{ON}	Ta= 25℃ (Relative To V_{DD})	V0 =15 V	-	1.6	2.0	KΩ	SEGn COMn *6
Oscillator Frequency	Internal Oscillator	fOSC	Ta = 25℃ 1/32Duty		2.286	2.54	2.794	kHz	CL
	External Input RECOMMAND	fCL			2.286	2.54	2.794		
Oscillator Frequency	Internal Oscillator	fOSC	Ta = 25℃ 1/64Duty		4.5	5	5.5	kHz	CL
	External Input RECOMMAND	fCL			4.5	5	5.5		

•Dynamic Consumption Current, During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used.

Display Pattern OFF

Ta = 25℃ Vout=17V

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
RW1065I	IDD	VDD=3.0 V, V0-Vss=8V	-	10	15	μA	*7
		VDD=5.0 V, V0-Vss=8V	-	35	45		

Display Pattern Checker

Ta = 25℃ Vout=17V

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
RW1065I	IDD	VDD=3.0 V, V0-Vss=8V	-	15	20	μA	*7
		VDD=5.0 V, V0-Vss=8V	-	40	50		

Display Pattern OFF

Ta = 25℃ Vout=17V

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
RW1065I	IDD	VDD=3.0 V, V0-Vss=8V	-	15	20	μA	*7
		VDD=5.0 V, V0-Vss=8V	-	40	50		

Display pattern Checker

Ta = 25℃ Vout=17V

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
RW1065I	IDD	VDD=3.0 V, V0-Vss=8V	-	65	80	μA	*7
		VDD=5.0 V, V0-Vss=8V	-	130	150		

• Consumption Current at Time of Power Saver Mode, VSS = 0 V, VDD = 3.0 V ± 10%

Item	Symbol	Condition	Rating			Unit	Notes
			Min.	Typ.	Max.		
Sleep mode	IDD	-	-	5	10	μA	-

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The D0, D1, D6, D7, CLS, CL, FR, M/S, and $\overline{RST}$ terminals.

*3 The D0, D1, D6, D7, $\overline{FR}$ and CL terminals.

*4 The CLS, M/S, and RST terminals.

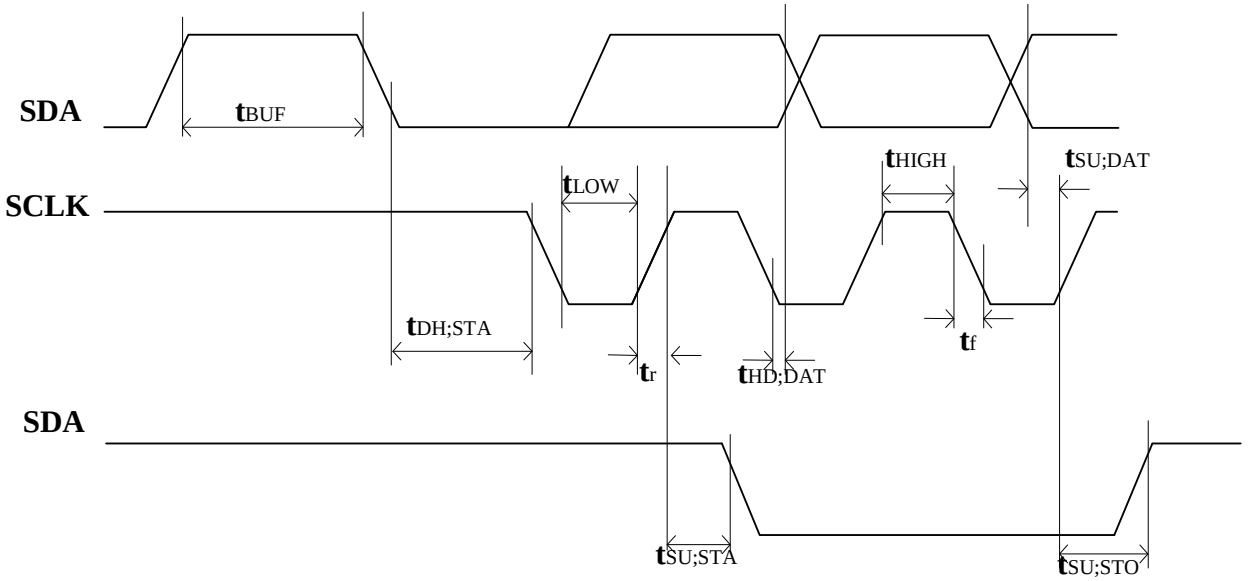
*5 Applies when the D0, D1, D6, D7, CL, and FR terminals are in a high impedance state.

*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminals SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage (3) range. RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*7 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on. Does not include the current due to the LCD panel capacity and wiring capacity. Applicable only when there is no access from the MPU.

■ TIMING CHARACTERISTICS

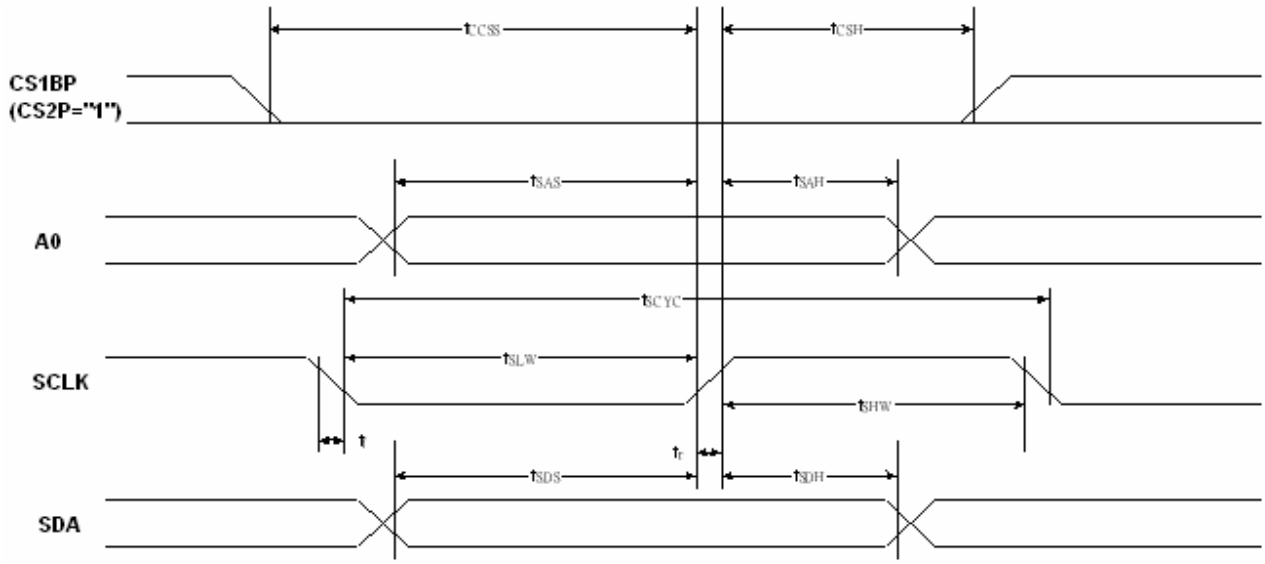
➢ IIC Interface



(Ta = 25°C)

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5V Rating		Units
				Min.	Max.	Min.	Max.	
SCLK clock frequency	SCLK	f_{SCLK}	—	DC	400	DC	400	KHz
SCLK clock low period		t_{LOW}		1.3	—	1.3	—	us
SCLK clock high period		t_{HIGH}		0.6	–	0.6	–	
Data set-up time	SDA	$t_{SU;DAT}$	—	180	–	80	–	ns
Data hold time		$t_{HD:DAT}$		0	0.9	0	0.9	us
SCLK,SDA rise time	SCLK, SDA	t_r	—	20+0.1C_b	300	20+0.1C_b	300	ns
SCLK,SDA fall time		t_f		20+0.1C_b	300	20+0.1C_b	300	
Capacitive load represent by each bus line		C_b	—	–	400	–	400	pf
Setup time for a repeated START condition	SDA	$t_{SU;STA}$	—	0.6	–	0.6	–	us
Start condition hold time		$t_{HD;STA}$	—	0.6	–	0.6	–	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	–	0.6	–	us
Bus free time between a Stop and START condition	SCLK	t_{BUF}	—	1.3	–	1.3	–	us

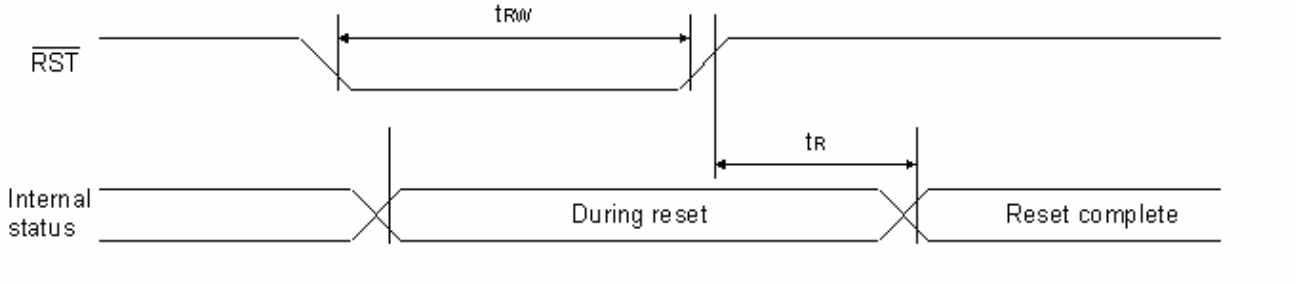
➢ 4-SPI serial interface



(Ta=25℃)

Item	Signal	Symbol	Condition	VDD=2.7V~4.5V Rating		VDD=4.5V~5.5V Rating		Units
				Min.	Min.	Max.	Max.	
Serial Clock Period	SCLK	tSCYC		50	50	—	—	ns
SCL “H” pulse width		tSHW		25	25	—	—	
SCL “L” pulse width		tSLW		25	25	—	—	
Address setup time	A0	tSAS		20	20	—	—	
Address hold time		tSAH		10	10	—	—	
Data setup time	SDA	tSDS		20	20	—	—	
Data hold time		tSDH		10	10	—	—	
CS-SCL time	CS1BP	tCSS		20	20	—	—	
CS-SCL time		tCSH		140	140	—	—	

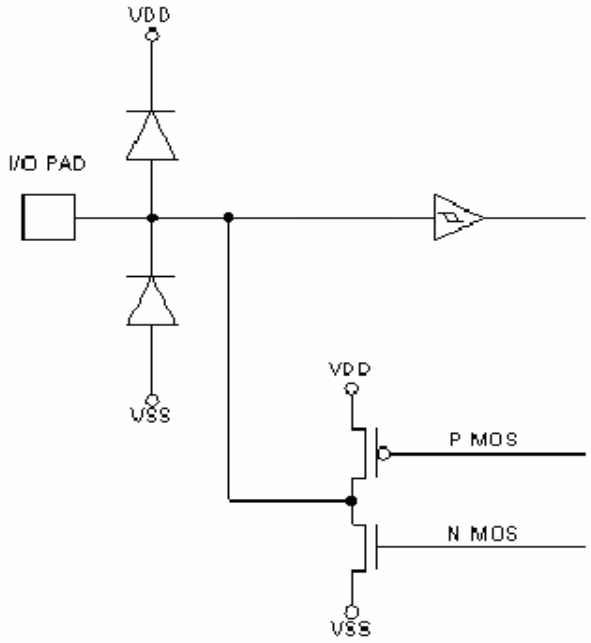
➢ Reset Timing



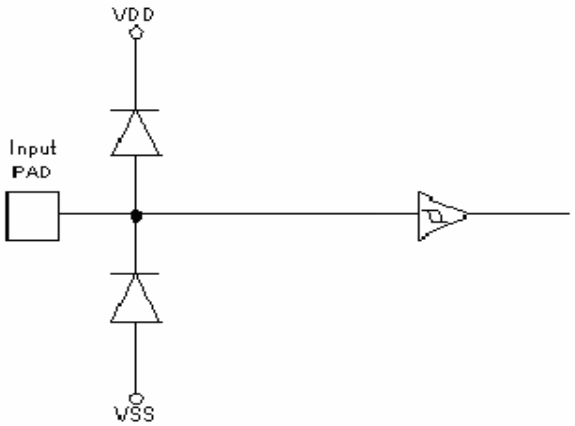
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time	—	t_R	—	—	-	2	μs
Reset “L” pulse width	RST	t_{RW}	—	2	-	—	μs

*1 When double chip was be used, then the duty set command must be set between the t_R

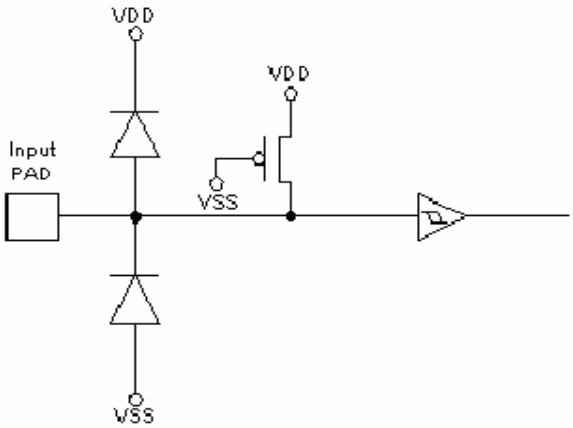
➢ I/O PAD CONFIGURATION



I/O PAD:D0,D1,D6,D7,FRR,CLL



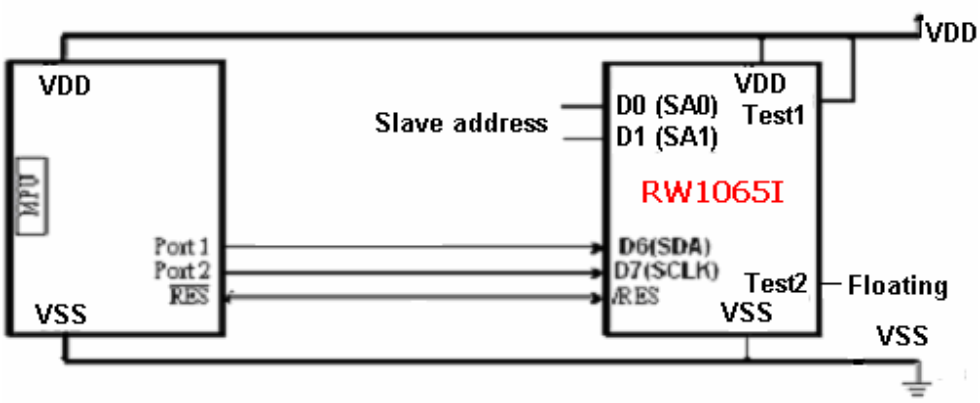
Input PAD:CLSP,M/S,BS0P,BS1P,ADCP,SHLP



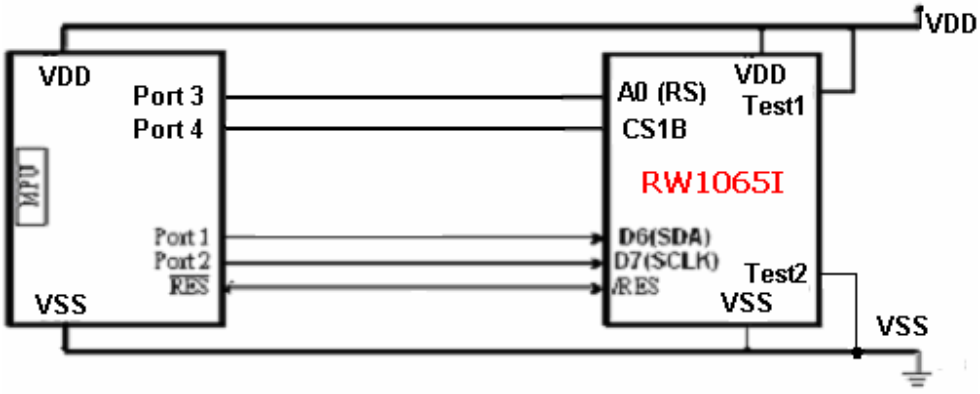
Input PAD:RSTP

■ THE MPU INTERFACE (REFERENCE EXAMPLES)

● IIC Serial Interface

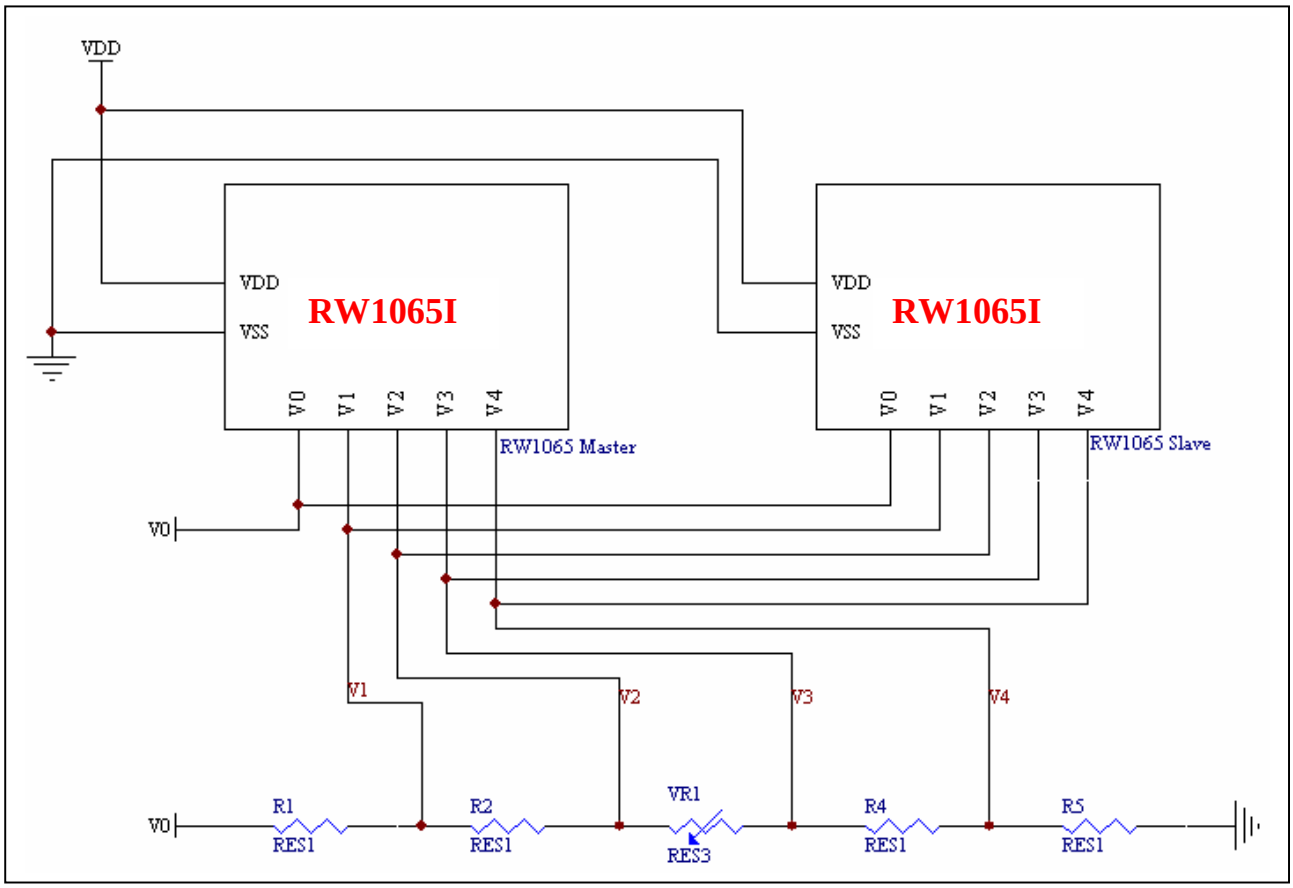


● 4-SPI Interface

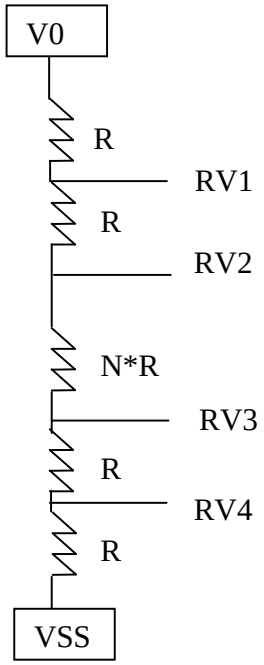


■ When using external multi-level power supply for LCD driving (REFERENCE EXAMPLE)

➢ Using a resistor divider can provide RW1065**I** external multi-level power supply for LCD driving. The circuit below shows a resistor divider network, which can bias V0, V1, V2, V3, and V4 externally



- Because pins can not set LCD bias when external power supplies are used for LCD driving, the bias can be set by an appropriate configuration for a resistor voltage divider networks. The example is shown below.



Bias Network Circuit Concept

1/5 Bias: N=1, total = 5R
1/6 Bias: N=2, total =6R
1/8 Bias: N=4, total =8R
1/9 Bias: N=5, total = 9R

•When V0, V1, V2, V3, and V4 are biased by external power supply, analog section of RW1065I should be turn off by software during LCD initialization. The example in below shows the sequence to turn off analog section when external bias is used.

Begin of LCD initialization

1. Reset RW1065I

2. SET EXT=1 (mode instruction)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	1

3. SET Display Command (double command)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	1
0	0	1	1	0	0	0	1

4. SET EXT=0 (mode instruction)

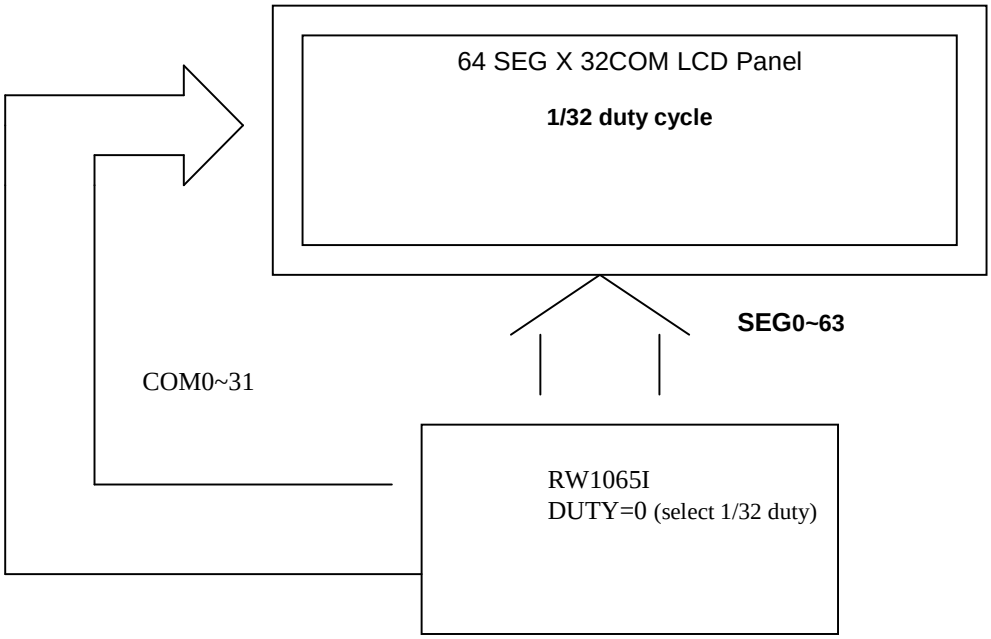
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	0

-
-

End of LCD initialization

■ Single chip solution for RW1065I application (REFERENCE EXAMPLE)

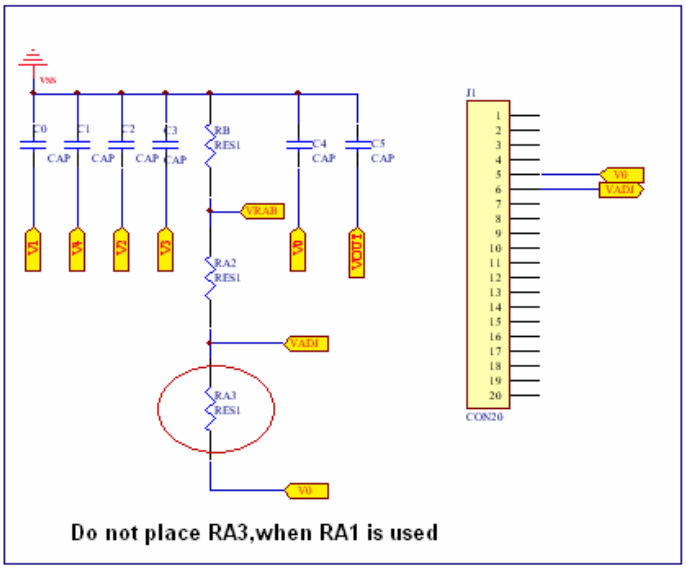
➢ For a 64x32 application, the duty cycle of LCD panel is 1/32 and the display duty of RW1065I should be set to 1/32. The display duty cycle can be selected by the DUTY bit in display command. The diagram for 64x32 applications is shown below.



■ Using an adjustable resistor on the main board to adjust the contrast of liquid crystal display (REFERENCE EXAMPLE)

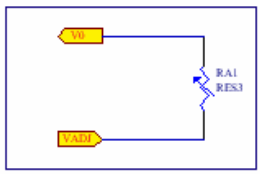
➢ The schematic shows an adjustable resistor on main board that can adjust voltage level of V0.

RW1065I LCD Module



Do not place RA3,when RA1 is used

Main Board



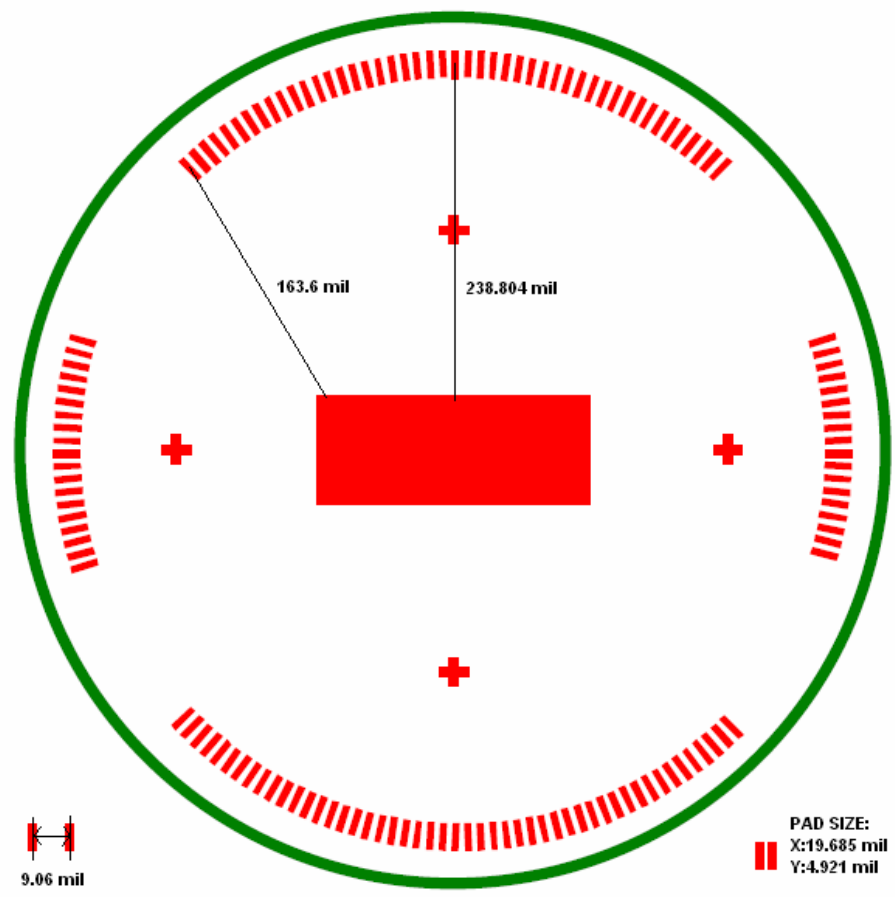
RA1 can adjust contrast of liqaid crystal display

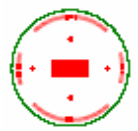
■ Package information:

(Please pay close attention to the information in this section. Do not hesitate to consult with our sale representative, if you have any question or concern.)

- In order to make better bonding yield for RW1065I; please follow the tips and recommendations in this section. In this section, few tips about COB footprint style, PCB layout, and wire bonding will be discussed.

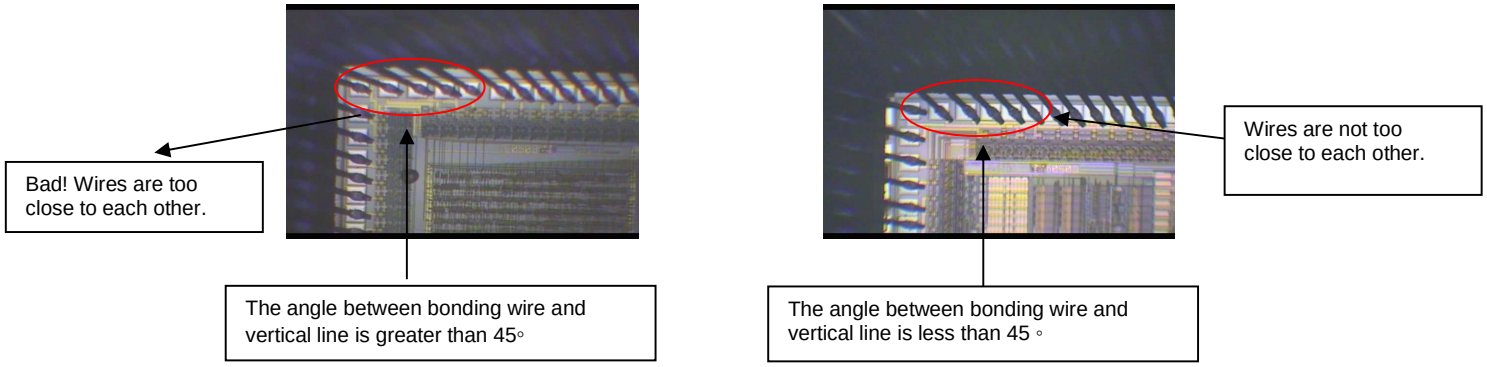
- The drawing in below shows the PCB footprint style, which we recommend for RW1065**I**. Pads array in curve shape is easier for Al wire bonding. Besides that, a real size COB footprint for RW1065**I** is also shown in below. RW1065**I** COB footprint is also available in powerpcb or protel format for design reference purpose.



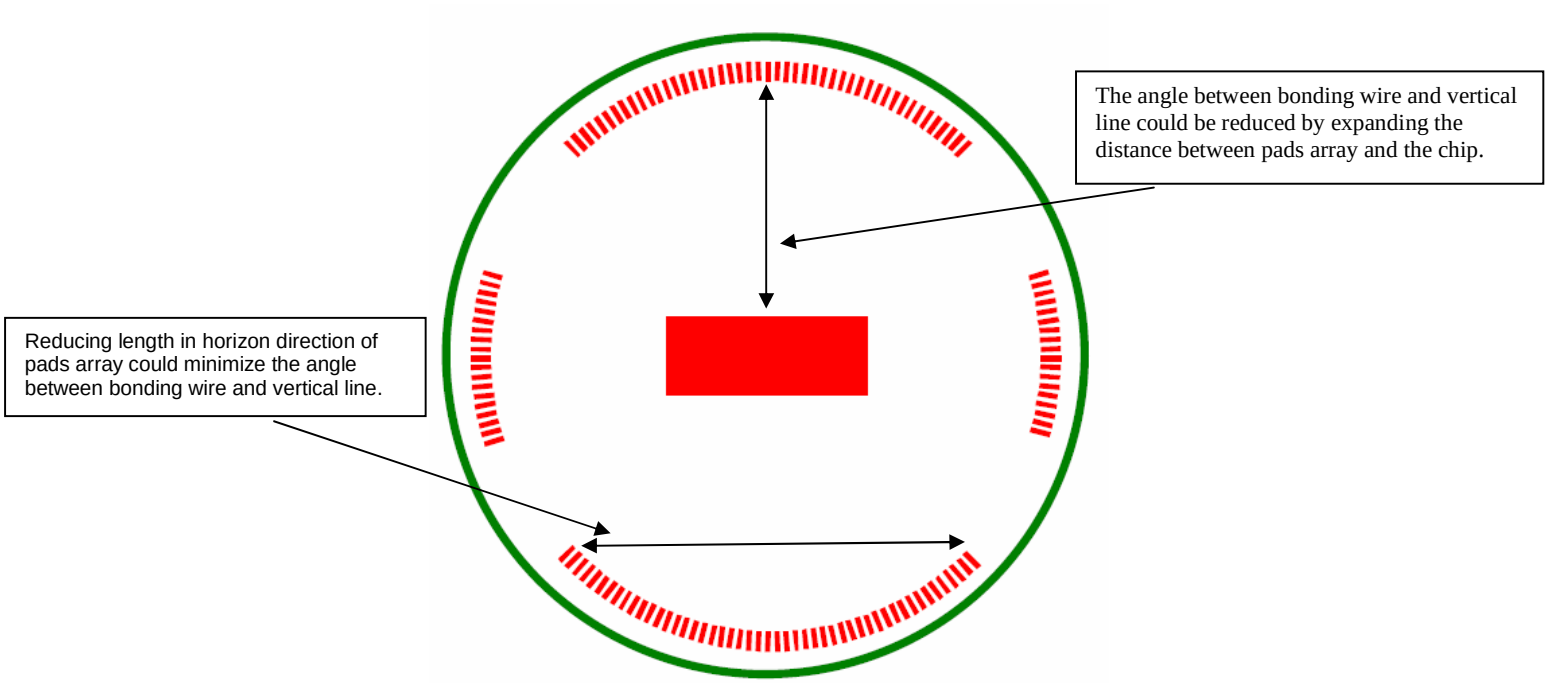


The ratio is 1:1

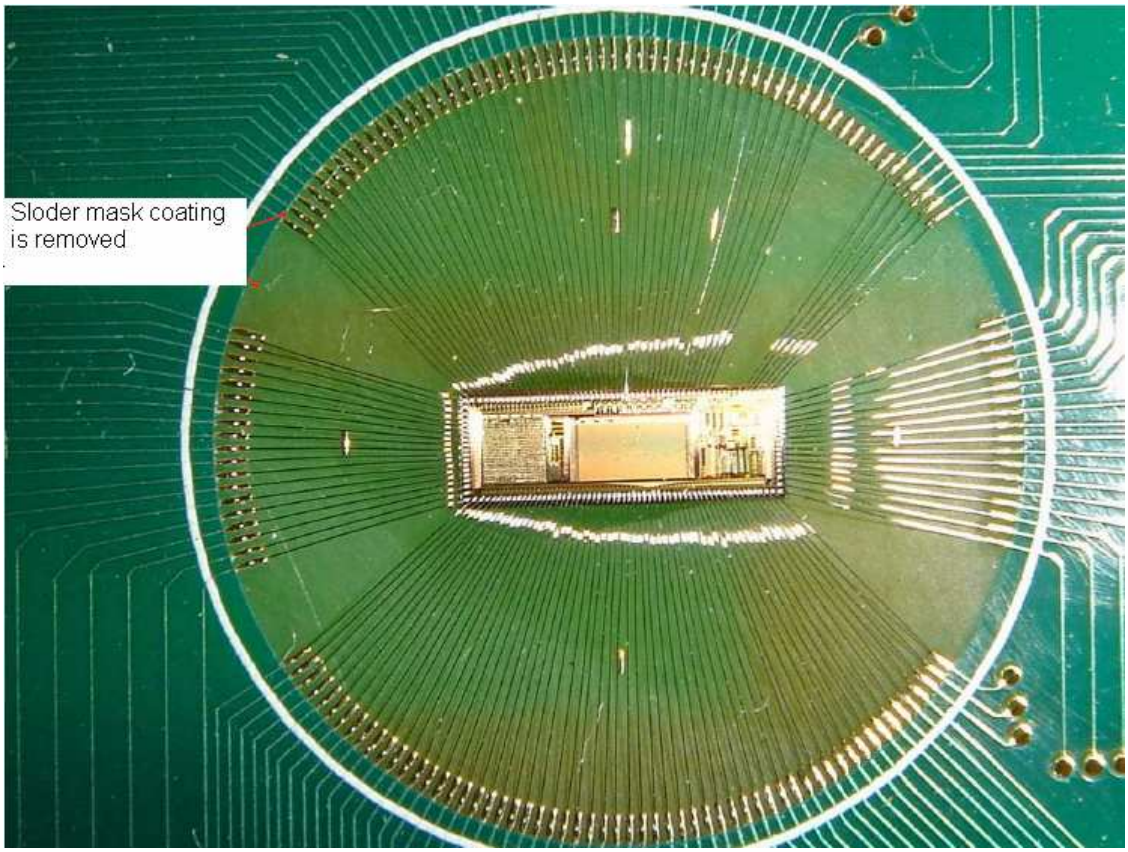
- During COB footprint design, there have some tips about footprint that the PCB designer should know. The angle between bonding wire and vertical line should less than 45 ◦. Otherwise, the wire shorts would become very easy to happen at fours corners of the chip.



- The angle between bonding wire and vertical line could be reduced by expanding the distance between pads array and the chip. In addition, reducing length in horizon direction of pads array could minimize the angle between bonding wire and vertical line. The picture in below will help to illustrate this concept. From the experiences, COB footprint style affects the bonding yield.



- If the gap between pads of COB footprint is filled with solder mask coating, it is difficult to bond Al wire to the pads. The top solder masks layer that overlap COB footprint area should be removed.



- Please use 1 mils diameter Al wire for RW1065**I** wire bonding.